The RISING Trigger

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In this document, we summarize the RISING trigger which has already been designed and implemented for the g-RISING experiments in 2005.

1 The concept of the trigger design

The general concept of the RISING trigger is very simple, i.e., using a logical AND signal between signals from a fast plastic scintillator at the FRS S4 area (usually sci41) and Ge detectors as a trigger signal to the DAQ system which runs with the MBS system [1, 2, 3]. For the fast-beam experiments, a logical AND is made between sci41 signals and prompt Ge signals, and a logical AND between delayed-stretched sci41 signals and delayed Ge signals is made for the stopped-beam experiments in order to reconstruct physical events of nuclear isomeric decays. In this document, we mainly describe the stopped-beam trigger, however, our trigger design also fits to the fast-beam experiments as described in the following sections.

Figure 1 shows the timing scheme of a *traditional* trigger method for a stopped-beam experiment. A fast logic signal from sci41 (a) is delayed by the time $T1$ and stretched by the time T2 shown as (b) in the figure. A typical value of $T1$ is an order of a few hundred ns in order to avoid prompt γ-flash events. The time $T2$ depends on the half-life of isomers of interest. This delayed-stretched signal creates a time window to the delayed-γ coincidence, which is called **γ-acceptance window**. A coincidence is made between (b) and Ge logic signals (c), thus the coincidence signal corresponds to delayed γ-ray events between the time $T1$ and $T1 + T2$. In the traditional way, gate signals to the digital modules including a common start signal for TDCs are created by an accepted trigger signals from the VME trigger module, therefore, the signal (d) can not be fed to the trigger module as a free trigger because the time of the signal (d) is not defined relative to the signal (a) (in the FRS electronics, all of measurements are done relative to the signal (a)). In order to create a time-defined free trigger to the VME trigger module, another coincidence must be made. A delayed signal made from the signal (a) is placed after the end-edge of the signal (b), shown as (f) in the figure, and the time distance between the end-edge of the signal (b) and the signal (f) is indicated as $T4$ in the figure. Another signal is made from (d), which is a stretched signal of (d), shown as (e) in the figure. The width of the signal, $T3$, is more than $T2 + T4$, therefore, the signal (e) always overlaps to the signal (f). A coincidence signal between (e) and (f) is now time-defined at $T5$, therefore, it is used as a free trigger signal to the VME trigger module. There are several disadvantages in this method, and the major disadvantage is caused by a huge delay of the free trigger signal. Since the gate signals to the digital electronics such as ADC. QDC and TDC are created by an accepted trigger signal from the VME trigger module in the traditional way, one has to put huge delay corresponding to the time $T5$ to all the analog signals to the digital electronics modules, especially for signals to QDC and TDC. If we change the time $T5$, all the analog signals must be re-adjusted. We think that this method is impractical for the RISING stopped-beam experiments, therefore, we have designed a trigger with **fast-gate delayed-trigger method with**

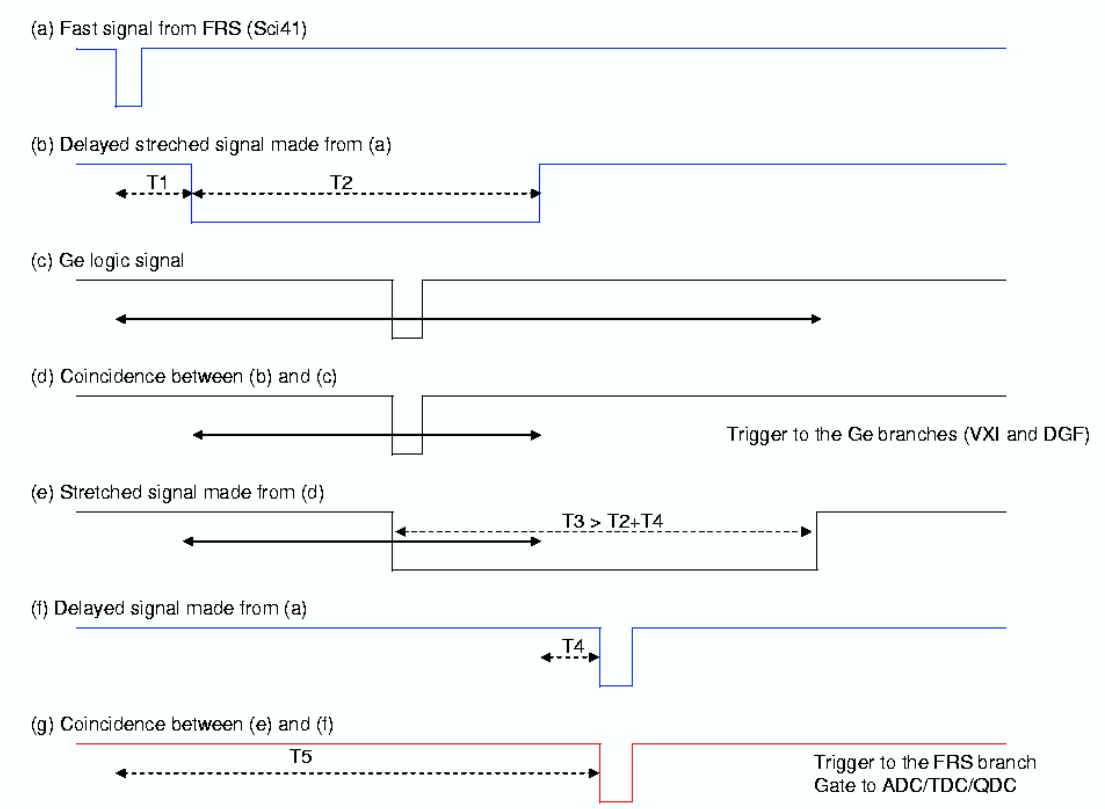

Figure 1: A traditional way of stopped-beam triggers, which will **NOT be used in the RISING experiments**.

FASTCLEAR, which will be described in the following sections. We consider the following major things for our trigger design,

- high flexibility,
- no interference to the FRS electronics and DAQ, i.e., delay of FRS analog signals is fixed for the both fast-beam and stopped-beam triggers with any change of the trigger delay condition,
- universal triggers for both fast-beam and stopped-beam experiments.

In the RISING fast beam experiments in 2004/2005, a stopped-beam trigger was implemented with *the fast-gate fast-trigger with FASTCLEAR* method, which is very similar to our proposed trigger here, in order to reconstruct isomer decay events for the secondary beam identification, and it was running smoothly, showing that the FASTCLEAR method really works.

2 Particle-γ coincidence trigger

In this section, the trigger which is used for the reconstruction of isomeric decay events is described.

2.1 Readout trigger for particle-γ coincidence

The first part of our proposed trigger scheme is very similar to the traditional trigger scheme in Figure 1, and it is shown in Figure 2. The fast signal from sci41 shown as (h) in Figure 2 is delayed by $T6$ and stretched by $T7$, creating the γ-acceptance window between the time $T6$ and $T6 + T7$ (the signal (i)). Ge logic signals (j) are produced by VME CFD modules in the DGF

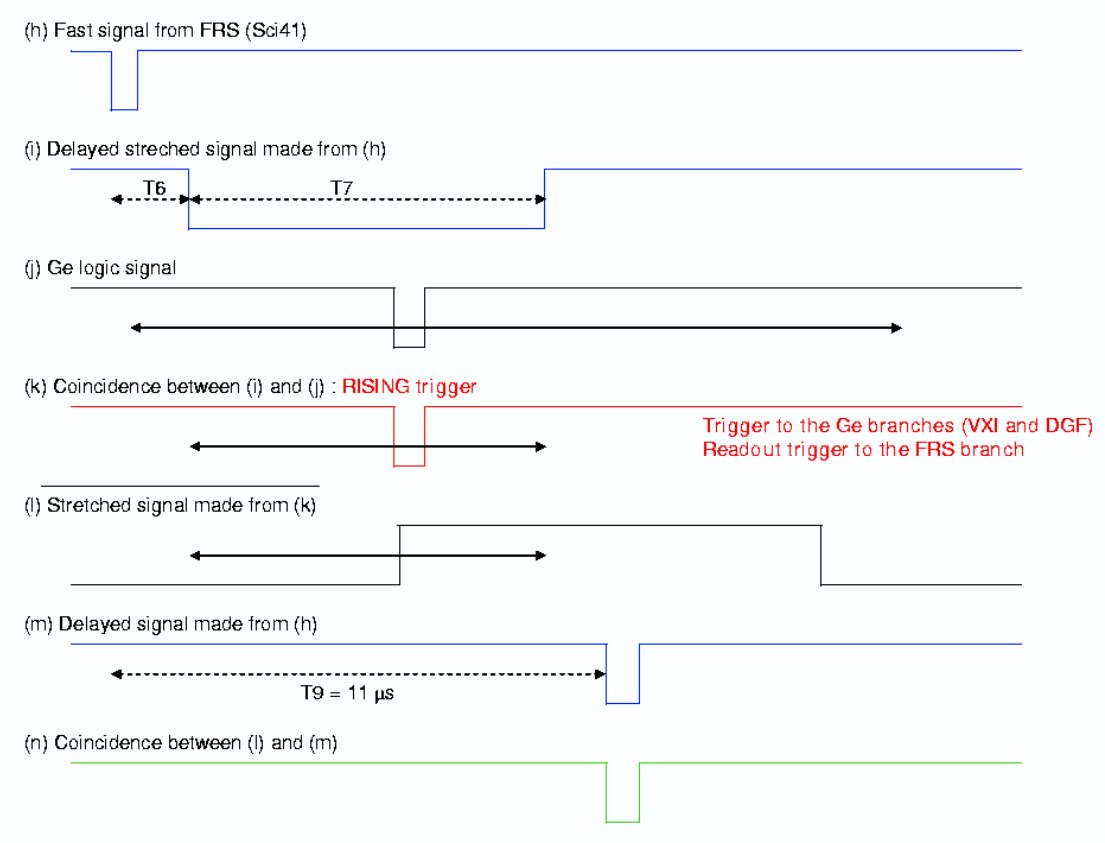

Figure 2: Timing scheme of the readout trigger and FASTCLEAR signals for the particle-γ coincidence events.

branch (**NOT VXI modules**) in our proposed trigger design. A coincidence between (i) and (j) is made in order to create particle-γ coincidence signals within the γ-acceptance window, shown as (k) in the figure. The signal (k) is so called **RISING trigger**, which is a **delayed-trigger**. In the current trigger design, the width of the γ-acceptance window can be varied up to 10 μs, however, we will modify the electronics to have a γ-acceptance widow up to 20 μs soon. This signal is fed to the VME trigger module in the FRS branch. The signal (k) is used only for the data readout request, but **the signal (k) is not used to create any gate signals to the FRS digital electronics** as described in the next subsection, because it is moving within the γ-acceptance window thus the time of the signal (k) is not defined. The RISING trigger signal (k) also goes to the DGF and VXI branched as a trigger.

In the RISING experiments, there are several DAQ branches (FRS, DGF, VXI and HECTOR branches) which run independently with common/different triggers, and the time-matching of the events among the different branches is done by using the GSI time-stamp module TITRIS [4]. Time-stamping is made with accepted trigger signals from the VME trigger module in the FRS, DGF and HECTOR branches and with validation signals in the VXI branch, which are created by the RISING trigger signal (k). In this scheme, the time-stamp difference between any of the branches is fixed within the TITRIS time resolution (within a few tens of ns) because the source of the time-stamp signals in all the branches are the signal (k) even though it is moving within the γ-acceptance window. If we employ the traditional way of the trigger described in the previous section, the time stamp difference is distributed within the period of the γ-acceptance window $T7$, thus the level of the background for the time-matching procedure is drastically increased.

2.2 GATE and FASTCLEAR signals for particle-γ coincidence

In order to avoid any interferences to the standard FRS electronics, the gate signals to the FRS digital electronics in the RISING experiments must be created in the same manner of the FRS electronics. Recently, the FRS group implemented the **fast-gate** method to create gate signals to the digital electronics, therefore, we also use the same method but with the FASTCLEAR technique described as follows.

The timing scheme for the GATE signals is shown in Figure 4. The RISING trigger (k) feeds into the VME trigger module in the FRS branches. The accepted trigger signal from the VME trigger module is produced in $\sim$ 600 ns after the signal (k). A VME Total-Dead-Time signal (T.D.T.) is also produced by the VME trigger module at the same time of the accepted trigger (signal (o)). The VME T.D.T. signal remains until the VME trigger module is ready for a next trigger signal. The time distance of the VME T.D.T. signal (o) to the RISING trigger (k) is approximately 600 ns. The T.D.T. signal is moving within the time amount of the γ-acceptance window $T7$ relative to the fast signal (h) because the the RISING trigger which is the source of the VME T.D.T. signal is moving in the γ-acceptance window.

We create a fast gate signal by the fast signal (h) but real T.D.T. inhibited because we must feed gate signals to the digital electronics only when the trigger can be accepted by the VME trigger module. A delayed signal made from the fast signal (h), the start-edge of which is shortly after the end-edge of the signal (h), is stretched widely enough to overlap to the start-edge of the VME T.D.T. signal (see signal (t)), and logic-bar of logic-OR of (o) and (t) is made as shown as the signal (u) in the figure, which is a real T.D.T. signal. When we make a coincidence between (h) and (u), we can produce a fast signal with real T.D.T. inhibited, the signal (v). The signal (v) must be stretched in order to cover the small gap between the signals (h) and (u). We can use this signal as a source of the gate signals to the VME ADC/QDC/TDC in the FRS branch. Since the VME T.D.T. signals move corresponding to the movement of the RISING trigger within the γ-acceptance window, the width of the signal (t) may proceed a few microseconds.

Since the RISING trigger is made by a coincidence between the delayed stretched sci41 signals and Ge logic signals, the RISING trigger do not coincide often to the fast gate signals. When the gate signal arrives to the digital electronics, the data conversion starts. By setting a proper FASTCLEAR WINDOW by a software, which is available in the CAEN digital VME modules, one can postpone the conversion process for the period of the FASTCLEAR window. The maximum FASTCLEAR window of CAEN modules is 39 μs. When the fast gate signal is fed into the VME modules but there is no readout trigger to the VME trigger module, the data stored in the digital electronics must be cleared. This process can be done by sending an ECL FASTCLEAR signal to the digital electronics within the FASTCLEAR WINDOW. The logic to produce the FASTCLEAR signals are shown in Figures 2 and 3. In the current trigger design, we create a delayed signal (m) made from (h) at 11 μs after the signal (h). The RISING trigger signal is stretched, the width of which must exceed 11 μs$-T6$ in order to always cover the signal (m) even though the trigger signal is moving in the γ-acceptance window, and then we make the logic-bar of the signal (see the signal (l)). When we make a coincidence between (l) and (m), there is a signal produced when trigger doesn't happen but when the gate signal is fed to the digital electronics (shown as (n)). The signal (n) can be used as a FASTCLEAR signal, however, the FASTCLEAR signal must also be real T.D.T. inhibited. The procedure to create a real T.D.T. inhibited FASTCLEAR signal is sketched in Figure 3. We create a delayed signal made from (n) shown as the signal (q) with a width exceeding the γ-acceptance window. Another delayed signal is made by the VME T.D.T. signal (o) the start-edge of which must always be shortly after the end-edge of the signal (q) (the signal is shown as (p) in th e figure). We just make logic-bar-OR of (p) and (q) (shown as (r)), and by making a coincidence between (n) and (r) it is obvious that a real T.D.T. inhibited FASTCLEAR

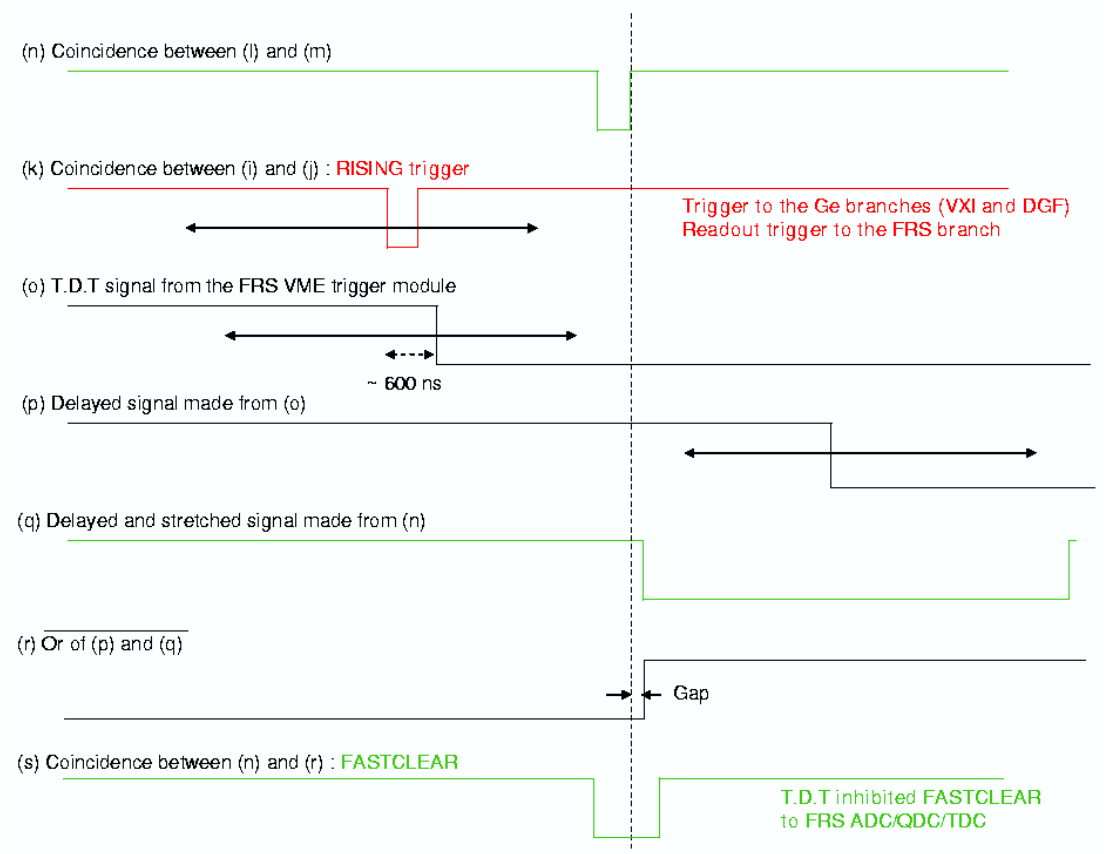

Figure 3: Timing scheme of the FASTCLEAR signals for the particle-γ coincidence events.

signals is produced. The signal (s) is of course stretched to cover the gap between the end-edge of (n) and the start-edge of (r). The signal (s) is fed into the FASTCLEAR input of all the digital VME modules except for the VME scaler in the FRS branch.

Since the timing of the gate signal (v) has the same timing of the gate signals used in the standard FRS DAQ system, we don't have to adjust the analog input signals to the digital electronics by putting delays, therefore, **the RISING part does not interfere to the FRS electronics**. We just have to activate the FASTCLEAR signals when we would like to use the RISING trigger.

3 Reduced FRS singles trigger

Since the RISING trigger is made by a coincidence between the fast sci41 signals and Ge logic signals, it is not a good trigger to monitor the beam profiles and the performance of particle detectors. Therefore, already since the beginning of the RISING fast beam campaign, we have been using a reduced sci41 signal by a factor 2^8 feeding to the FRS DAQ as a trigger. This type of the trigger is so called *Reduced FRS singles trigger*.

Figures 5, 6 and 7 shows the timing scheme for the reduced FRS singles trigger. Reduced FRS singles signals with a reduction factor of 2^8 (the factor can be varied as 2^n, n is an integer value) are produced by the GSI NIM trigger box. The reduced FRS singles trigger signal is a delayed one of the reduced signal placed at 5 μs after the fast sci41 signal (h) (see the signal (w)). The reduced FRS singles trigger is provided usually only to the FRS branch in the fast beam experiments, but it can be of course fed to the DGF and VXI branches if needed. The gate signals for the reduced FRS

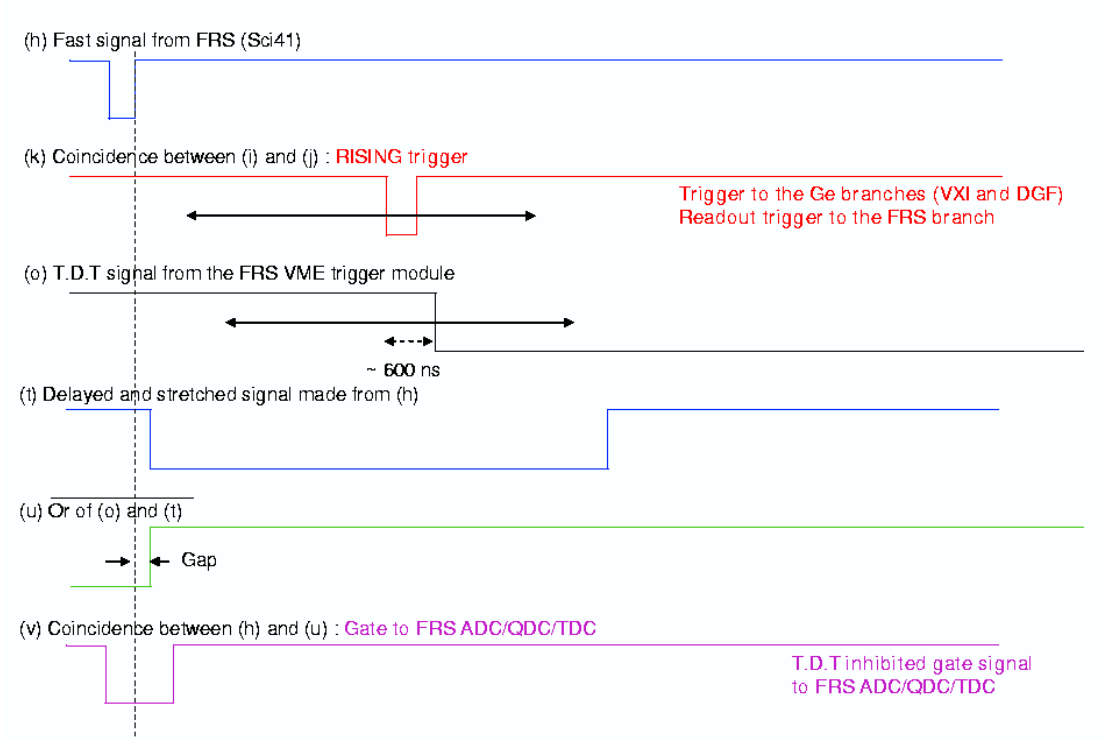

Figure 4: Timing scheme of the GATE signals for the particle-γ coincidence events.

singles trigger is created in the same way for the particle-γ coincidence trigger as shown in Figure 7.

Each particle firing sci41 contributes to create the gate signal, while the FRS reduced singles trigger is produced every 2^8 sci41 signals, therefore, FASTCLEAR signal must also be fed to the FRS digital electronics when the reduced FRS singles trigger doesn't coincide to the gate signal. The FASTCLEAR signal is produced in the same manner for the particle-γ coincidence trigger, and it is shown in Figures 5 and 6.

4 Random trigger

Since stopped-beam experiments should use a wide γ-acceptance window in order to reconstruct events of isomeric decays, large random particle-γ coincidence probability is expected. Therefore, very careful investigation on the random coincidence background including background subtraction must be conducted in the data analysis. Therefore, we have already prepared triggers for random coincidence events. The trigger logic can be obviously same for the particle-γ coincidence trigger shown in Figures 2, 3 and 4. There is only one difference, i.e., the fast signal from sci41 (h) is replaced by a logic signal from the random pulser.

5 Trigger tagging

The GSI VME trigger module has four trigger inputs, therefore, the trigger type can be tagged at the VME trigger modules bit-wise with four bits (16 different triggers). The trigger type is appeared in the MBS event header. In the standard FRS DAQ system, the trigger type appears as 1, therefore, different types of our triggers (particle-γ coincidence trigger, reduced FRS singles trigger, random trigger and the time-calibrator trigger: the time-calibrator trigger is not described in this document). Therefore, the trigger type is tagged by using the FRS digital electronics. The

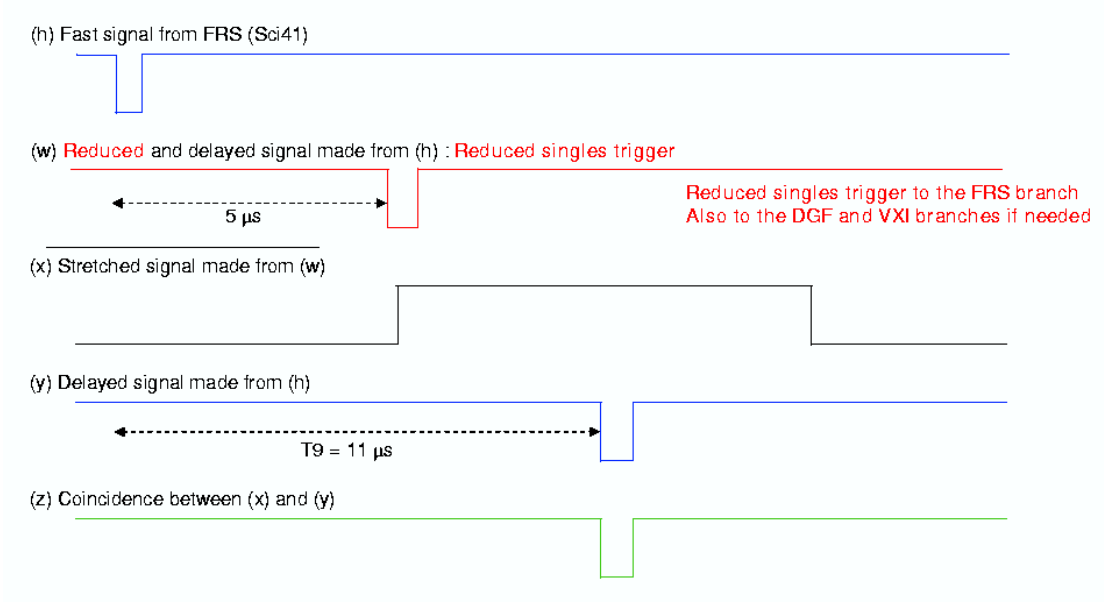

Figure 5: Timing scheme of the readout trigger and FASTCLEAR signals for the reduced FRS singles coincidence events.

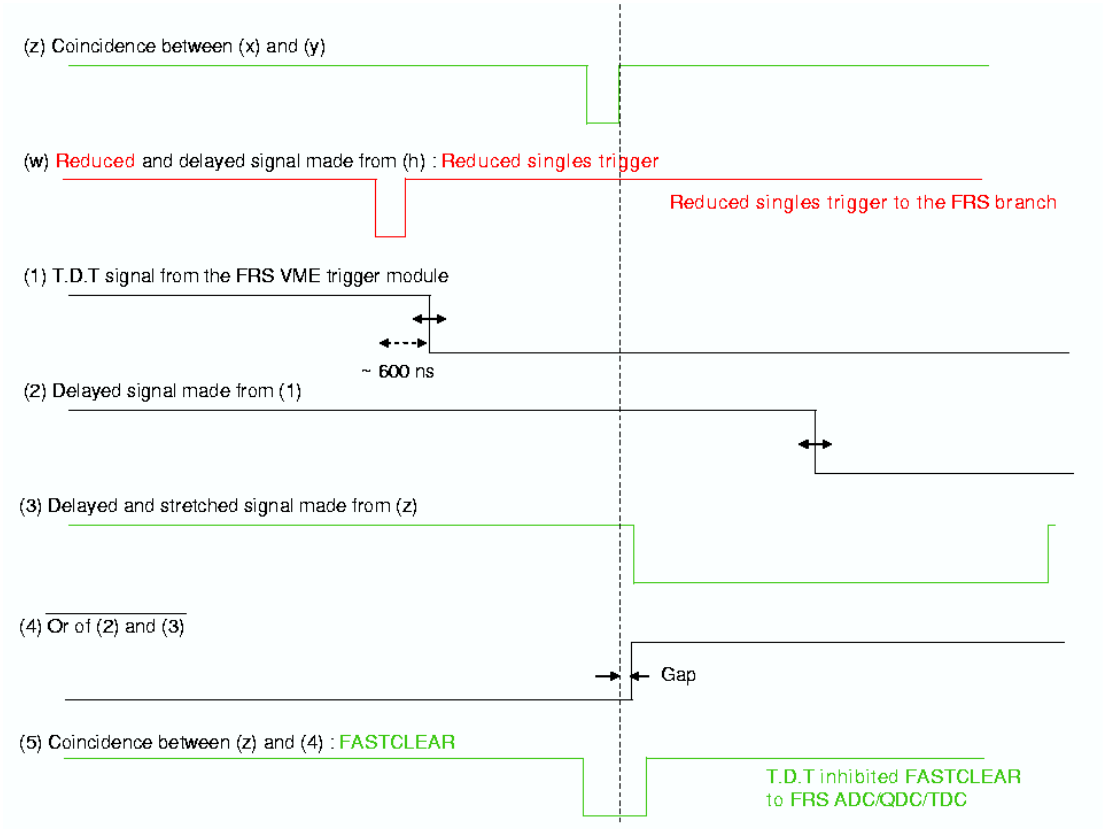

Figure 6: Timing scheme of the FASTCLEAR signals for the reduced FRS singles events.

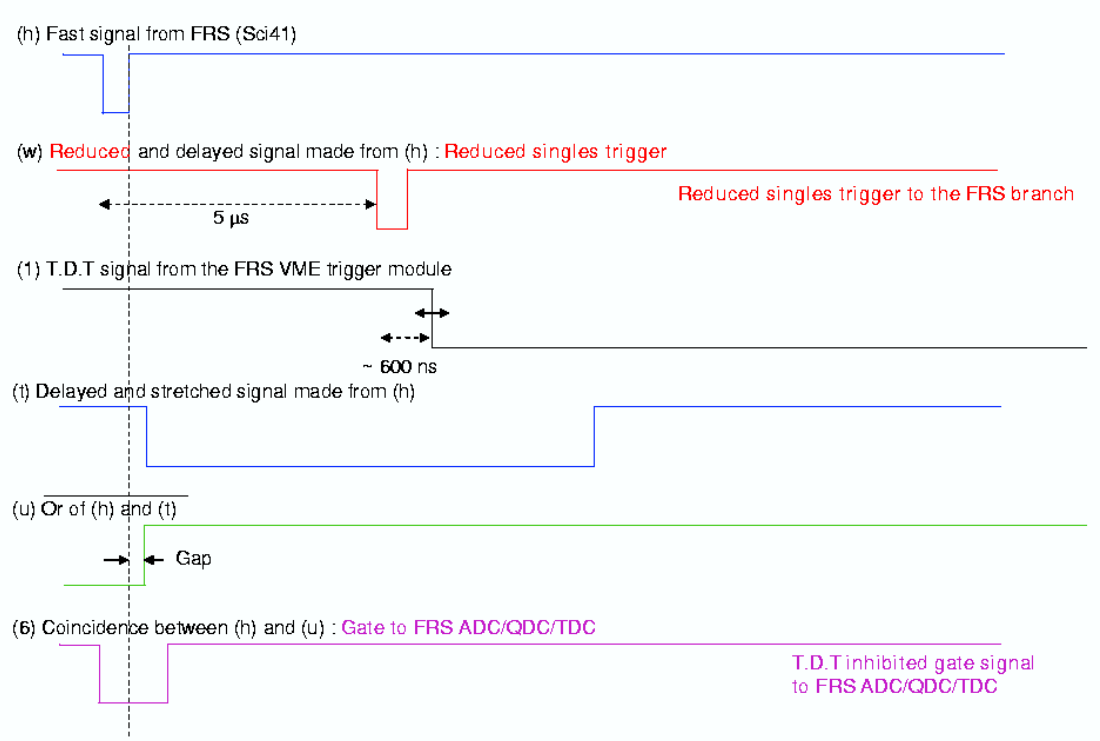

Figure 7: Timing scheme of the GATE signals for the reduced FRS singles events.

source signals of each trigger type, which is properly adjusted, are fed to the different channels of the FRS VME ADC at the slot number 17 (the list of the channels can be obtained soon). **In the analysis, the trigger type must be selected by requesting the presence of the ADC data word in the corresponding ADC channel, otherwise, one doesn't know the trigger type**. This must also be done in the online monitoring, otherwise the analysis is contaminated by random coincidence events in the different trigger types. The trigger tagging in the fast beam experiment was also done in the same manner (also using FRS VME TDC), and the data analysis on the fast-beam experiments also needs the trigger selection, as stated previously many times.

6 Time measurement

The lifetime measurement of isomeric states can be done in two steps in the current RISING system in principle.

The time difference between the fast sci41 signal (h) ($T = 0$) and the RISING trigger signal (k) is measured by a NIM TAC module, and analog pulses from the TAC is fed to the FRS VME ADC at the slot number 17. Since the timing of the RISING trigger is defined by the Ge logic signal from the DGF branch (see Figure 2), the TAC signal gives information on the time difference between the fast sci41 signal (h) and the Ge logic signal. The timing of Ge logic signals from the DGF branch is defined by the fastest signal arrives to the VME CFD in the DGF branch, therefore, we essentially measure the time of the fastest Ge fired (of course the delay in the cables and modules is considered) relative to the fast sci41 signal. Since the timing of the trigger signals fed to the DGF and VXI branches are defined by the fastest Ge signal, the time measurement in the DGF and VXI branches can be made only relative to the fastest Ge signals within the time window of the DGF and VXI systems (in the DGF branch, the time measurement is made by VME TDCs). It is clear in the argument above that the time information of the second Ge signal in the same event will

be missed if the the time distance between the first and second Ge signals exceeds the width of the time window in the DGF and VXI systems, and this fact must be considered as clearly stated in the g-RISING meeting at GSI in July. From our point of view, most (all?) of the experiments could not be bothered by this fact if the analysis is done properly.

7 Deadtime

The concept of the stopped-beam trigger system may give impression that we may induce huge deadtime due to the wide γ-acceptance window and wide FASTCLEAR window, however, it is not true. For example, in the FRS branch, one must be aware that one channel of VME electronics modules needs approximately 1 μs readout time. The deadtime of the FRS DAQ is typically 150 μs, depending on the number of the channels to be readout. In our trigger design, we have only 20 μs deadtime if we set the FASTCLEAR window as 20 μs, which will induce only $\sim$13 % more deadtime relative to the one in the standard FRS DAQ system. Without having the FASTCLEAR window, the additional deadtime will be defined by the γ-acceptance window, which will induce 10 μs more deadtime anyway, and cannot be avoided in any of stopped-beam trigger scheme.

8 Application to the fast-beam experiments

In this document, we present the stopped-beam trigger, however, our trigger design also fits to the fast-beam experiments. Therefore, our trigger design can be used as **the universal RISING trigger**. In the fast-beam experiments, prompt Ge logic signals (j) in Figure 2 must be stretched approximately by 500 ns, and a delayed signal made from the fast sci41 signal (h) must be put within the stretched Ge logic signal. A coincidence signal between the stretched Ge logic signal and the delayed sci41 signal is fed to all the branches as a RISING fast-beam readout trigger. Gate and FASTCLEAR signals are created in the same manner discussed in the previous sections, therefore, the standard FRS electronics can be used without any interference.

9 Restriction

The time separation between a gate signal and the next one should be more than the FASTCLEAR window, otherwise the deadtime is increased. For example, the rate of the fast signal (h) is somehow limited to be 50 k Hz if the FASTCLEAR window is 20 μs. This rate corresponds to the rate of sci41 for the RISING trigger. We usually do not meet this rate because our beam intensity at sci41 is limited to be below because of the rate capability restriction of an ionization chamber such as MUSIC at S4.

References

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