MVME197IG/D1A1
May 1994

Supplement to

MVME197DP and MVME197SP

Single Board Computers

Installation Guide

(MVME197IG/D1)

The attached pages are replacements and/or additions to the installation guide. They correct minor errors and update some features.

Please replace the pages according to the following table and place this page behind the title page of the installation guide as a record of this change:

Replace Old	With New
v/vi,	v/vi,
1-1 through 1-4,	1-1 through 1-4,
1-7 through 1-10	1-7 through 1-10

- A vertical bar (|) in the margin of a replacement page indicates a text change or addition.
- The supplement number is shown at the bottom of each replacement page.

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Related Documentation

The following publications are applicable to the MVME197 module series and may provide additional helpful information. If not shipped with this product, they may be purchased by contacting your Motorola sales office.

Document Title	Motorola Publication Number
MVME197LE Single Board Computer User's Manual	MVME197LE
MVME197LE Single Board Computer Support Information	SIMVME197LE
MVME197DP and MVME197SP Single Board Computer User's Manual	MVME197
MVME197DP and MVME197SP Single Board Computer Support Information	SIMVME197
MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide	MVME197PG
MVME197BUG 197Bug Debugging Package User's Manual	MVME197BUG
MVME197BUG 197Bug Diagnostic Firmware User's Manual	MVME197DIAG
MVME712M Transition Module and P2 Adapter Board User's Manual	MVME712M
MVME712-12, MVME712-13, MVME712A, MVME712AM, and MVME712B Transition Module and LCP2 Adapter Board User's Manual	MVME712A
MC68040/MC68EC040/MC68CL040 Microprocessor User's Manual	M68040UM/AD
MC88110 Second Generation RISC Microprocessor User's Manual	MC88110UM/AD
MC88410 Secondary Cache Controller User's Manual	MC88410UM/AD

Notes

1. **The support information manuals (SIMVME197LE and SIMVME197) contain: the connector interconnect signal information, parts lists, and the schematics for the specific board(s) indicated.**

2. **Although not shown in the above list, each Motorola Computer Group manual publication number is suffixed with characters which represent the revision level of the document, such as "/D2" (the second revision of a manual); a supplement bears the same number as the manual but has a suffix such as "/A1" (the first supplement to the manual).**

To further assist your development effort, Motorola has collected user's manuals for each of the peripheral controllers used on the MVME197 module series and other boards from the suppliers. This bundle includes manuals for the following:

68-1X7DS for use with the MVME197 series of Single Board Computers.

NCR 53C710 SCSI Controller Data Manual and Programmer's Guide
Intel i82596 Ethernet Controller User's Manual
Cirrus Logic CD2401 Serial Controller User's Manual
SGS-Thompson MK48T08 NVRAM/TOD Clock Data Sheet

The following non-Motorola publications may also be of interest and may be obtained from the sources indicated. The VMEbus Specification is contained in ANSI/IEEE Standard 1014-1987.

ANSI/IEEE Std 1014-1987 Versatile Backplane Bus: VMEbus	The Institute of Electrical and Electronics Engineers, Incorporated Publication and Sales Department 345 East 47th Street New York, New York 10017-2633 Telephone: 1-800-678-4333
ANSI Small Computer System Interface-2 (SCSI-2), Draft Document X3.131-198X, Revision 10c	Global Engineering Documents P.O. Box 19539 Irvine, California 92713-9539 Telephone (714) 979-8135

BOARD LEVEL HARDWARE DESCRIPTION 1

Introduction

This chapter describes the board level hardware features of the MVME197DP and MVME197SP versions of the MVME197 series of Single Board Computers, hereafter referred to as the MVME197, unless separately specified (refer to the next section for model designations).

The chapter is organized with a board level overview and features listed in this introduction, followed by a more detailed hardware functional description. Front panel switches and indicators are included in the detailed hardware functional description. This chapter closes with some general memory maps.

All programmable registers used in the MVME197 module series reside in ASIC (Application-Specific Integrated Circuit) devices that are covered in the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide*.

Model Designations

The MVME197DP/SP module series of the Single Board Computers are available in the following models.

Table 1-1. MVME197DP/SP Model Designations

Model Number	Motorola Part Number	Model Description
MVME197SP series		
MVME197-101	01-W3815B04	Single Processor MC88110, 256KB Cache, 128MB Onboard ECC DRAM, 50 MHz
MVME197DP series		
MVME197-201	01-W3815B03	Dual Processor MC88110, 256KB Cache per Processor, 128MB Onboard ECC DRAM, 50 MHz

Overview

Each MVME197 module is a double-high VMEmodule based on the MC88110 RISC (Reduced Instruction Set Computing) microprocessor.

The MVME197DP/SP module series have 128/256MB of onboard DRAM with programmable ECC (Error Checking and Correction), 256KB of external cache memory for **each** MC88110/MC88410 microprocessor/cache controller combination (note that the MVME197SP version has only one MC88110/MC88410 device combination), 4MB of flash memory, 8KB of static RAM (with battery backup), a time of day clock (with battery backup), an Ethernet transceiver interface, four serial ports with EIA-232-D interface, six tick timers, a watchdog timer, 256KB of BOOT ROM, a SCSI bus interface with DMA (Direct Memory Access), a Centronics printer port, an A16/A24/A32/D8/D16/D32 VMEbus master/slave interface, and a VMEbus system controller.

Input/Output (I/O) signals are routed through the MVME197's backplane connector P2. A P2 Adapter Board or LCP2 Adapter board routes the signals and grounds from connector P2 to an MVME712 series transition module. The MVME197 supports the MVME712M, MVME712A, MVME712AM, and MVME712B transition boards (referred to here as the MVME712X, unless separately specified). The MVME197 also supports the MVME712-12 and MVME712-13 (referred to as the MVME712-XX, unless separately specified). These transition boards provide configuration headers, serial port drivers, and industry standard connectors for the I/O devices.

The MVME197 modules have eight ASIC devices (described in the following order: BusSwitch, DCAM, ECDM, PCC2, and VME2).

Note **For the MVME197 series, the term Local Bus, as used in other MVME1xx Single Board Computer series, is referred to as the Local Peripheral Bus.**

The BusSwitch ASIC provides an interface between the processor bus (MC88110/410 bus) and the local peripheral bus (MC68040 compatible bus). Refer to the board specific MVME197 block diagram (Figure 1-1 and 1-2). It provides bus arbitration for the MC88410 bus and serves as a seven level interrupt handler. It has programmable map decoders for both busses, as well as write post buffers on each, two tick timers, and four 32-bit general purpose registers.

The DCAM (DRAM Controller and Address Multiplexer) ASIC provides the address multiplexers and RAS/CAS/WRITE control for the DRAM as well as data control for the ECDM.

The ECDM (Error Correction and Data Multiplexer) ASIC multiplexes between four data paths on the DRAM array. Since the device handles 16 bits, four such devices are required on the MVME197 to accommodate the 64-bit data bus of the MC88110 RISC microprocessor. Single-bit error correction and double-bit detection is performed in the ECDM.

The PCCchip2 (Peripheral Channel Controller) ASIC provides two tick timers and the interface to the LAN chip, the SCSI chip, the serial port chip, the printer port, and the BBRAM (Battery Backup RAM).

The VMEchip2 ASIC provides a VMEbus interface. The VMEchip2 includes two tick timers, a watchdog timer, programmable map decoders for the master and slave interfaces, and a VMEbus to/from the local peripheral bus DMA controller, a VMEbus to/from the local peripheral bus non-DMA programmed access interface, a VMEbus interrupter, a VMEbus system controller, a VMEbus interrupt handler, and a VMEbus requester.

The local peripheral bus to VMEbus transfers can be D8, D16, or D32. VMEchip2 DMA transfers to the VMEbus, however, can be 64 bits wide as Block Transfer (BLT).

Requirements

All MVME197 boards are designed to conform to the requirements of the following documents:

- ❏ VMEbus Specification (IEEE 1014-87)
- ❏ EIA-232-D Serial Interface Specification, EIA
- ❏ SCSI Specification, ANSI

Features

These are some of the major features of the MVME197DP/SP single board computers:

- ❏ Single MC88110 RISC Microprocessor with an MC88410 Cache Controller (MVME197SP module series)
- ❏ Dual MC88110 RISC Microprocessors, each with one MC88410 Cache Controller (MVME197DP module series)
- ❏ 256 kilobytes of external cache per processor, controlled by the MC88410 (MVME197DP and MVME197SP module series)
- ❏ 128 or 256 megabytes of 64-bit Dynamic Random Access Memory (DRAM) with Error Checking and Correction (ECC)

- ❏ 4 megabytes of Flash memory
- ❏ Six status LEDs (FAIL, RUN, SCON, LAN, SCSI, and VME)
- ❏ 8 kilobytes of Static Random Access Memory (SRAM) and Time of Day (TOD) clock with Battery Backup RAM (BBRAM)
- ❏ Two push-button switches (ABORT and RESET)
- ❏ 256 kilobytes of BOOT ROM
- ❏ Six 32-bit tick timers for periodic interrupts
- ❏ Watchdog timer
- ❏ Eight software interrupts
- ❏ I/O
  - SCSI Bus interface with Direct Memory Access (DMA)
  - Four serial ports with EIA-232-D buffers
  - Centronics printer port
  - Ethernet transceiver interface
- ❏ VMEbus interface
  - VMEbus system controller functions
  - VMEbus interface to local peripheral bus (A24/A32, D8/D16/D32 BLT (D8/D16/D32/D64))(BLT = Block Transfer)
  - Local peripheral bus to VMEbus interface (A24/A32, D8/D16/D32 BLT (D16/D32/D64))
  - VMEbus interrupter
  - VMEbus interrupt handler
  - Global CSR for inter-processor communications
  - DMA for fast local memory - VMEbus transfers (A16/A24/A32, D16/D32 BLT (D16/D32/D64))

Specifications

The specifications for the MVME197DP/SP are listed in the following table.

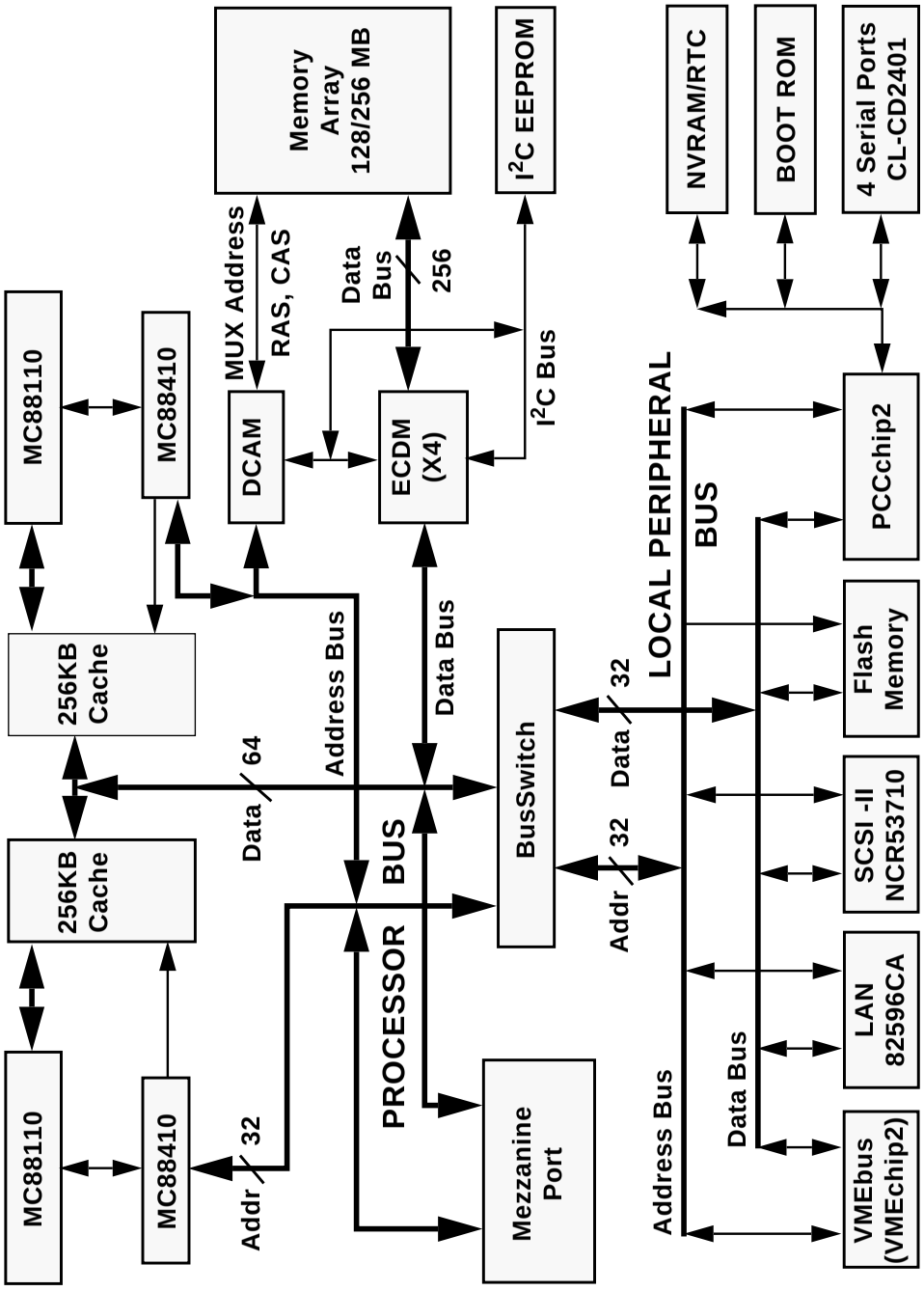

Figure 1-2. MVME197DP Block Diagram

Functional Description

The following sections contain a functional description of the major blocks on the MVME197DP/SP single board computers.

Front Panel Switches and Indicators

There are two push-button switches and six LEDs on the front panel of the MVME197. The switches are RESET and ABORT. The RESET switch (S3) will reset all onboard devices and drive the SYSRESET* signal if the board **is** the system controller. The RESET switch (S3) will reset all onboard devices except the DCAM and ECDM if the board **is not** the system controller. The VMEchip2 generates the SYSRESET* signal. The BusSwitch combines the VMEchip2 local reset, the power up reset, and the reset switch to generate a local board reset. Refer to the *Reset Module* section in the *BusSwitch* chapter of the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide* for more information.

The ABORT switch (S2) can generate an interrupt to CPU0 via the NMI* signal. It is normally used to abort program execution and return to the debugger. This capability is controlled via the ABORT register in the BusSwitch. Refer to the *BusSwitch* chapter of the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide* for more information.

The six LEDs on the MVME197 front panel are: FAIL, SCON, RUN, LAN, VME, and SCSI.

1. The yellow FAIL LED (DS1) is lit when the BRDFAIL signal line is active.
2. The green SCON LED (DS2) is lit when the VMEchip2 is the VMEbus system controller.
3. The green RUN LED (DS3) is lit when the MC88110 bus MC* pin is low.
4. The green LAN LED (DS4) lights when the LAN chip is the local peripheral bus master.
5. The green VME LED (DS5) lights when the board is using the VMEbus or when the board is accessed by the VMEbus.
6. The green SCSI LED (DS6) lights when the SCSI chip is the local peripheral bus master.

Data Bus Structure

The data bus structure is arranged to accommodate the various 8-bit, 16-bit, 32-bit, and 64-bit devices that reside on the module. Refer to the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide* and to the user's guide for each device to determine its port size, data bus connection, and any restrictions that apply when accessing the device.

MC88110 MPU

The MVME197 series of single board computers are based on the MC88000 families of RISC (Reduced Instruction Set Computer) microprocessors. Depending on the specific MVME197 module, the MVME197 series uses the MC88110 RISC microprocessor. Refer to the *Module Designation* section in the beginning of this chapter for MVME197 module/processor variations and to the *MC88110 Second Generation RISC Microprocessor User's Manual* for more detailed information on this device.

MC88410 Cache Controller

Depending on the specific MVME197DP/SP module version, each MC88110 microprocessor is connected directly to an MC88410 Secondary Cache Controller. Each MC88410 controls a 256KB level two cache. Refer to the *MC88410 Secondary Cache Controller User's Manual* and the *MCM62110 Data Sheet* for more information on this device.

BOOT ROM

The board accommodates a 32-pin PLCC/CLCC ROM/EPROM referred to as BOOT ROM or DROM (Download ROM). It is organized as a 256K x 8 device, but as viewed from the processor it looks like a 32K x 64 memory. This memory is mapped starting at location $FFF80000, but after a local reset it is also mapped at location 0, providing a reset vector and bootstrap code for the processor. The DR0 bit in the General Control Register (GCR) of the PCCchip2 must be cleared to disable the BOOT ROM memory map at 0. In addition, the ROM0 bit in the ROMCR register of the BusSwitch must be cleared.

Flash Memory

4MB of flash memory is available on the board. Flash memory works like EPROM, but can be erased and reprogrammed by software. It is organized as 32 bits wide, but to the processor it looks as 64 bits wide. It is mapped at location $FF800000. Reads can be of any size, including burst transfers, but writes are always 32 bits wide, regardless of the size specified for the transfer.

For this reason, software should only use 32-bit write transfers. This memory is controlled by the BusSwitch, and the memory size, access time, and write enable capability can be programmed via the ROM Control Register (ROMCR) in the BusSwitch. The flash memory can be accessed from the processor bus only. It is not accessible from the local peripheral bus or VMEbus.

Onboard DRAM

The onboard DRAM on the MVME197DP/SP (2 banks of 128MB memory, one optionally installed) is sized at 128MB using 4M x 4 devices and configured as 256 bits wide.

The DRAM is four-way interleaved to efficiently support cache burst cycles. The DRAM is controlled by the DCAM and ECDM, and the map decoders in the DCAM can be programmed through the I^2C bus interface in the ECDM to accommodate different base address(es) and sizes. The onboard DRAM is not disabled by a local peripheral bus reset. Refer to the *DCAM* and *ECDM* chapters in the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide* for detailed programming information.

Battery Backup RAM and Clock

The MK48T08 RAM and clock chip is used on the MVME197. This chip provides a time of day clock, oscillator, crystal, power fail detection, memory write protection, 8KB of RAM, and a battery in one 28-pin package. The clock provides seconds, minutes, hours, day, date, month, and year in BCD 24-hour format. Corrections for 28-, 29-, (leap year) and 30-day months are automatically made. No interrupts are generated by the clock. The MK48T08 is an 8-bit device; however the interface provided by the PCCchip2 supports 8-, 16-, and 32-bit accesses to the MK48T08. Refer to the *PCCchip2* chapter in the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide* and to the MK48T08 data sheet for detailed programming information.

VMEbus Interface

The local peripheral bus to VMEbus interface, the VMEbus to local peripheral bus interface, and the local-VMEbus DMA controller functions on the MVME197 are provided by the VMEchip2. The VMEchip2 can also provide the VMEbus system controller functions. Refer to the *VMEchip2* chapter in the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide* for detailed programming information.