MVME197LEIG/D1A2
May 1994

Supplement to

MVME197LE

Single Board Computer

Installation Guide

(MVME197LEIG/D1)

The attached pages are replacements and/or additions to the installation guide. They correct minor errors and update some text.

Place this page behind the title page of the installation guide as a record of this change. Please replace the pages according to the following table:

Replace Old	With New
v/vi, 1-1/1-2, 1-5/1-6, 1-13 through 1-16	v/vi, 1-1/1-2, 1-5/1-6, 1-13 through 1-16

- A vertical bar (|) in the margin of a replacement page indicates a text change or addition.
- The supplement number is shown at the bottom of each replacement page.

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Related Documentation

The following publications are applicable to the MVME197 module series and may provide additional helpful information. If not shipped with this product, they may be purchased by contacting your Motorola sales office.

Document Title	Motorola Publication Number
MVME197LE Single Board Computer User's Manual	MVME197LE
MVME197LE Single Board Computer Support Information	SIMVME197LE
MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide	MVME197PG
MVME197BUG 197Bug Debugging Package User's Manual	MVME197BUG
MVME197BUG 197Bug Diagnostic Firmware User's Manual	MVME197DIAG
MVME712M Transition Module and P2 Adapter Board User's Manual	MVME712M
MVME712-12, MVME712-13, MVME712A, MVME712AM, and MVME712B Transition Module and LCP2 Adapter Board User's Manual	MVME712A
MC68040/MC68EC040/MC68CL040 Microprocessor User's Manual	M68040UM/AD
MC88110 Second Generation RISC Microprocessor User's Manual	MC88110UM/AD

Notes

1. **The support information manual (SIMVME197LE) contains: the interconnect signal information, parts lists, and the schematics for the specific board indicated.**
2. **Although not shown in the above list, each Motorola Computer Group manual publication number is suffixed with characters which represent the revision level of the document, such as "/D2" (the second revision of a manual); a supplement bears the same number as the manual but has a suffix such as "/A1" (the first supplement to the manual).**

To further assist your development effort, Motorola has collected user's manuals for each of the peripheral controllers used on the MVME197 module series and other boards from the suppliers. This bundle includes manuals for the following:

68-1X7DS for use with the MVME197 series of Single Board Computers.

NCR 53C710 SCSI Controller Data Manual and Programmer's Guide
Intel i82596 Ethernet Controller User's Manual
Cirrus Logic CD2401 Serial Controller User's Manual
SGS-Thompson MK48T08 NVRAM/TOD Clock Data Sheet

The following non-Motorola publications may also be of interest and may be obtained from the sources indicated. The VMEbus Specification is contained in ANSI/IEEE Standard 1014-1987.

ANSI/IEEE Std 1014-1987 Versatile Backplane Bus: VMEbus	The Institute of Electrical and Electronics Engineers, Incorporated Publication and Sales Department 345 East 47th Street New York, New York 10017-2633 Telephone: 1-800-678-4333
ANSI Small Computer System Interface-2 (SCSI-2), Draft Document X3.131-198X, Revision 10c	Global Engineering Documents P.O. Box 19539 Irvine, California 92713-9539 Telephone (714) 979-8135

BOARD LEVEL HARDWARE DESCRIPTION 1

Introduction

This chapter describes the board level hardware features of the MVME197LE Single Board Computer. The chapter is organized with a board level overview and features listed in this introduction, followed by a more detailed hardware functional description. Front panel switches and indicators are included in the detailed hardware functional description. This chapter closes with some general memory maps.

All programmable registers in the MVME197LE module reside in ASIC (Application-Specific Integrated Circuit) devices that are covered in the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide*.

Overview

The MVME197LE module is a double-high VMEmodule based on the MC88110 RISC (Reduced Instruction Set Computing) microprocessor. The MVME197LE has 32/64MB of DRAM, 1MB of flash memory, 8KB of static RAM (with battery backup), a time of day clock (with battery backup), an Ethernet transceiver interface, four serial ports with EIA-232-D interface, six tick timers, a watchdog timer, 128KB of BOOT ROM, a SCSI bus interface with DMA (Direct Memory Access), a Centronics printer port, an A16/A24/A32/D8/D16/D32 VMEbus master/slave interface, and a VMEbus system controller.

Input/Output (I/O) signals are routed through the MVME197LE's backplane connector P2. A P2 Adapter Board or LCP2 Adapter board routes the signals and grounds from connector P2 to an MVME712 series transition module. The MVME197LE supports the MVME712M, MVME712A, MVME712AM, and MVME712B transition boards (referred to here as the MVME712X, unless separately specified). The MVME197LE also supports the MVME712-12 and MVME712-13 (referred to as the MVME712-XX, unless separately specified). These transition boards provide configuration headers, serial port drivers, and industry standard connectors for the I/O devices.

The MVME197LE modules have eight ASIC devices (described in the following order: BusSwitch, DCAM, ECDM, PCC2, and VME2).

The BusSwitch ASIC provides an interface between the processor bus (MC88110 bus) and the local peripheral bus (MC68040 compatible bus). Refer to the MVME197LE block diagram (Figure 1-1). It provides bus arbitration for the MC88110 bus and serves as a seven level interrupt handler. It has programmable map decoders for both busses, as well as write post buffers on each, two tick timers, and four 32-bit general purpose registers.

The DCAM (DRAM Controller and Address Multiplexer) ASIC provides the address multiplexers and RAS / CAS / WRITE control for the DRAM as well as data control for the ECDM.

The ECDM (Error Correction and Data Multiplexer) ASIC multiplexes between four data paths on the DRAM array. Since the device handles 16 bits, four such devices are required on the MVME197LE to accommodate the 64-bit data bus of the MC88110 microprocessor. Single-bit error correction and double-bit detection is performed in the ECDM.

The PCCchip2 (Peripheral Channel Controller) ASIC provides two tick timers and the interface to the LAN chip, the SCSI chip, the serial port chip, the printer port, and the BBRAM (Battery Backup RAM).

The VMEchip2 ASIC provides a VMEbus interface. The VMEchip2 includes two tick timers, a watchdog timer, programmable map decoders for the master and slave interfaces, and a VMEbus to / from the local peripheral bus DMA controller, a VMEbus to / from the local peripheral bus non-DMA programmed access interface, a VMEbus interrupter, a VMEbus system controller, a VMEbus interrupt handler, and a VMEbus requester.

The local peripheral bus to VMEbus transfers can be D8, D16, or D32. VMEchip2 DMA transfers to the VMEbus, however, can be 64 bits wide as Block Transfer (BLT).

Requirements

These boards are designed to conform to the requirements of the following documents:

- ❏ VMEbus Specification (IEEE 1014-87)
- ❏ EIA-232-D Serial Interface Specification, EIA
- ❏ SCSI Specification, ANSI

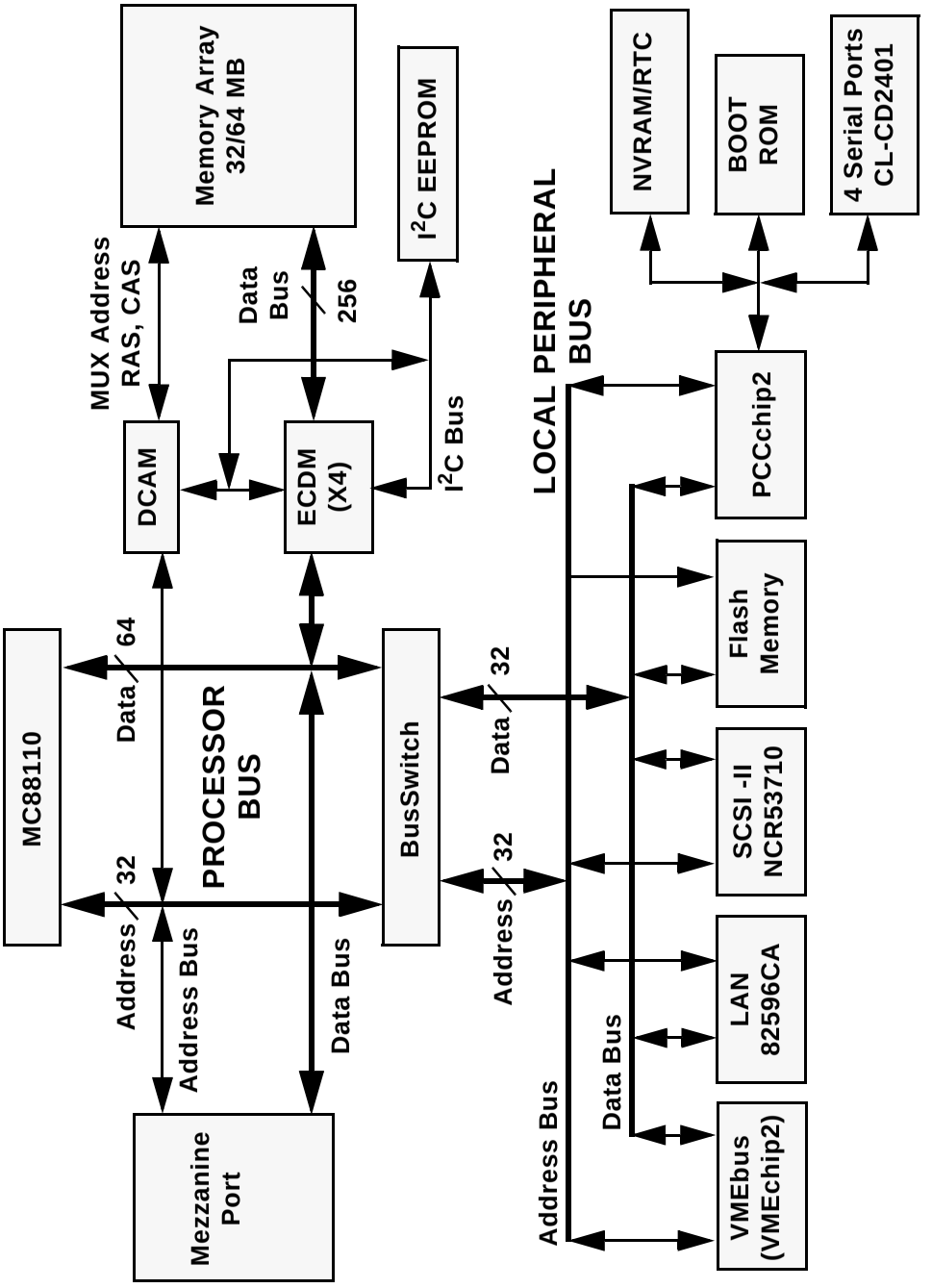

Figure 1-0. MVME197LE Block Diagram

Functional Description

The following sections contain a functional description of the major blocks on the MVME197LE single board computer.

Front Panel Switches and Indicators

There are two push-button switches and six LEDs on the front panel of the MVME197LE module. The switches are RESET and ABORT. The RESET switch (S3) will reset all onboard devices and drive the SYSRESET* signal if the board **is** the system controller. The RESET switch (S3) will reset all onboard devices except the DCAM and ECDM if the board **is not** the system controller. The VMEchip2 generates the SYSRESET* signal. The BusSwitch combines the local reset and the reset switch to generate a local board reset. Refer to the *Reset Driver* section in the *VMEchip2* chapter of the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide* for more information.

When enabled by software, the ABORT switch (S2) generates an interrupt at a user-programmable level. It is normally used to abort program execution and return to the debugger. Refer to the *VMEchip2* chapter of the *MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide* for more information.

The six LEDs on the MVME197LE front panel are: FAIL, SCON, RUN, LAN, VME, and SCSI.

1. The yellow FAIL LED (DS1) is lit when the BRDFAIL signal line is active.
2. The green SCON LED (DS2) is lit when the VMEchip2 is the VMEbus system controller.
3. The green RUN LED (DS3) is lit when the MC88110 bus MC* pin is low.
4. The green LAN LED (DS4) lights when the LAN chip is the local peripheral bus master.
5. The green VME LED (DS5) lights when the board is using the VMEbus or when the board is accessed by the VMEbus.
6. The green SCSI LED (DS6) lights when the SCSI chip is the local peripheral bus master.

The memory maps of MVME197LE devices are provided in the following tables. Table 1-2 is the entire map from $00000000 to $FFFFFFFF. Many areas of the map are user-programmable, and suggested uses are shown in the table. This is assuming no address translation is used between the processor and local peripheral bus and between the local peripheral bus and VMEbus. The cache inhibit function is programmable in the MC88110. The onboard I/O space must be marked cache inhibit and serialized in its page table. Table 1-3 further defines the map for the local devices.

Table 1-2. Processor Bus Memory Map

Address Range	Devices Accessed	Port Size	Size	Software Cache Inhibit	Notes
$00000000 - (DRAMSIZE -1)	User Programmable (Onboard DRAM)	D64	DRAMSIZE	N	1
DRAMSIZE - $FF7FFFFF	User Programmable (VMEbus)	D32/D16	3GB	?	2,3
$FF800000 - $FFBFFFFF	Flash Memory	D32	4MB	N	5
$FFC00000 - $FFEFFFFF	reserved	---	3MB	---	4
$FFF00000 - $FFFEFFFF	Local Devices (Refer to next table)	D32-D8	1MB	Y	---
$FFFF0000 - $FFFFFFFF	User Programmable (VMEbus A16)	D32/D16	64KB	?	1,3

Notes

1. **This area is user-programmable. The suggested use is shown in the table. The DRAM decoder is programmed in the DCAM through the ECDM I^2C bus interface. The Processor Bus to Local Peripheral Bus and the Local Peripheral Bus to Processor Bus decoders are programmed in the BusSwitch. The Local Peripheral to VMEbus (master) and VMEbus to Local Peripheral Bus (slave) decoders are programmed in the VMEchip2.**
2. **Size is approximate.**
3. **Cache inhibit depends on devices in area mapped.**
4. **This area is not decoded. If these locations are accessed and the local peripheral bus timer is enabled, the cycle times out and is terminated by a TEA signal.**
5. **This area is user programmable via the BusSwitch. Default size is 4 megabytes.**

The following table focuses on the Local Devices portion of the Memory Map.

Table 1-3. Local Devices Memory Map

Address Range	Devices Accessed	Port Size	Size	Notes
$FFF00000 - $FFF00FFF	BusSwitch	D64-D8	4KB	1
$FFF01000 - $FFF01FFF	ECDM (DCAM access)	---	4KB	1
$FFF02000 - $FFF02FFF	reserved	---	4KB	4
$FFF03000 - $FFF03FFF	reserved	---	4KB	4
$FFF04000 - $FFF04FFF	reserved	---	4KB	4
$FFF05000 - $FFF05FFF	reserved	---	4KB	4
$FFF06000 - $FFF06FFF	reserved	---	4KB	4
$FFF07000 - $FFF07FFF	User defined	---	4KB	4
$FFF08000 - $FFF3FFFF	reserved	---	224KB	4
$FFF40000 - $FFF400FF	VMEchip2 (LCSR)	D32	256B	1,2,3
$FFF40100 - $FFF401FF	VMEchip2 (GCSR)	D32-D8	256B	1,2,3
$FFF40200 - $FFF40FFF	reserved	---	3.5KB	4,5
$FFF41000 - $FFF41FFF	reserved	---	4KB	4
$FFF42000 - $FFF42FFF	PCCchip2	D32-D8	4KB	1,2
$FFF43000 - $FFF43FFF	reserved	---	4KB	4
$FFF44000 - $FFF44FFF	reserved	---	4KB	3
$FFF45000 - $FFF45FFF	CD2401 (Serial Comm. Cont.)	D16-D8	4KB	1,2
$FFF46000 - $FFF46FFF	82596CA (LAN)	D32	4KB	1,2,6
$FFF47000 - $FFF47FFF	53C710 (SCSI)	D32 / D8	4KB	1,2
$FFF48000 - $FFF4FFFF	reserved	---	32KB	4
$FFF50000 - $FFF6FFFF	reserved	---	128KB	4
$FFF70000 - $FFF77FFF	reserved	---	32KB	4
$FFF78000 - $FFF7FFFF	reserved	---	288KB	4
$FFF80000 - $FFFBFFFF	DROM (BOOT ROM)	---	256KB	7
$FFFC0000 - $FFFCFFFF	MK48T08 (BBRAM,TOD Clk)	D32-D8	64KB	1,2
$FFFD0000 - $FFFEFFFF	reserved	---	128KB	4

Notes

1. **For a complete description of the register bits, refer to the appropriate data sheet for the specific chip. For a more detailed memory map refer to the detailed peripheral device memory maps in the MVME197LE, MVME197DP, and MVME197SP Single Board Computers Programmer's Reference Guide.**

2. **Address is the physical address going to the device. It is after the BusSwitch translation from the MC88110 address to the device seen address.**
3. **Writes to the LCSR in the VMEchip2 must be 32 bits. LCSR writes of 8 or 16 bits terminate with a TEA signal. Writes to the GCSR may be 8, 16, or 32 bits. Reads to the LCSR and GCSR may be 8, 16, or 32 bits.**
4. **This area does not return an acknowledge signal. If the processor bus timeout timer is enabled, the access times out and is terminated by a TEA signal.**
5. **Size is approximate.**
6. **Port commands to the 82596CA must be written as two 16-bit writes: upper word first and lower word second.**
7. **DROM (BOOT ROM) appears at $0 following a local peripheral bus reset. The DROM appears at 0 until the DR0 bit is cleared in the PCCchip2. In addition, the ROM0 bit in the ROMCR register of the BusSwitch must be cleared before the DRAM is accessed.**

VMEbus Memory Map

This section describes the mapping of local resources as viewed by VMEbus masters.

VMEbus Accesses to the Local Peripheral Bus

The VMEchip2 includes a user-programmable map decoder for the VMEbus to local peripheral bus interface. The map decoder allows the user to program the starting and ending address and the modifiers the MVME197LE responds to.

VMEbus Short I/O Memory Map

The VMEchip2 includes a user-programmable map decoder for the GCSR (Global Control and Status Registers). The GCSR map decoder allows the user to program the starting address of the GCSR in the VMEbus short I/O space.