MVME197PG/D1A1
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Supplement to

MVME197LE, MVME197DP, and MVME197SP

Single Board Computers

Programmer's Reference Guide

(MVME197PG/D1)

The attached pages are replacements for the corresponding pages in the manual. Place this page behind the title page of the manual as a record of this change. Please replace the pages according to the following table:

Replace Old	With New	Add New
iii/iv, ix/x thru xxiii/xxiv 1-1/1-2, 1/3-1-4, 1-5/1-6, 1-7/1-8, 1-13/1-14, 1-15/1-16 thru 1-25/1-26, 2-1/2-2 thru 2-3/2-4, 2-17/2-18 thru 2-19/2-20, 2-25/2-26 thru 2-27/2-28, 2-31/2-32 thru 2-37/2-38, 2-41/2-42 thru 2-45/2-46, 2-49/2-50, 2-53/2-54, 2-63/2-64 thru 2-65/2-66, 2-89/2-90 thru 2-91/2-92, 2-95/2-96	iii/iv, ix/x thru xxiii/xxiv 1-1/1-1.a and 1-1.b/1-2, 1-3/1-3.a and 1-3.b/1-4, 1-5/1-5.a and 1-5.b/1-6, 1-7/1-8, 1-13/1-13a and 1-13.b/1-14, 1-15/1-16 thru 1-25/1-26, 2-1/2-2 thru 2-3/2-4, 2-17/2-18 thru 2-19/2-20, 2-25/2-26 thru 2-27/2-28, 2-31/2-32 thru 2-37/2-38, 2-41/2-42 thru 2-45/2-46, 2-49/2-50, 2-53/2-54, 2-63/2-64 thru 2-65/2-66, 2-89/2-90 thru 2-91/2-92, 2-95/2-96	1-6.a/1-6.b,

Replace Old	With New	Add New
3-1/3-2, 3-3/3-4, 3-7/3-8 thru 3-9/3-10, 3-13/3-14, 3-17/3-18 thru 3-19/3-20, 3-27/3-28, 3-31/3-32 thru 3-33/3-34 3-45/3-46, 4-1/4-2, 4-3/4-4 thru 4-13/4-14, 4-15/4-16, 4-19/4-20, 4-23/4-24 thru 4-29/4-30, 4-33/4-34, 4-37/4-38, 4-39/4-40, 4-41/4-42, 5-1/5-2 thru 5-3/5-4, 5-9/5-10 thru 5-11/5-12, 5-17/5-18, 5-25/5-26, 6-1/6-2 thru 6-3/6-4, 6-9/6-10 thru 6-17/6-18, 6-23/6-24 thru 6-25/6-26, IN-1/IN-2 thru IN-15/IN-16	3-1/3-2, 3-3/3-3.a and 3-3.b/3-4, 3-7/3-8 thru 3-9/3-10, 3-13/3-14, 3-17/3-18 thru 3-19/3-20, 3-27/3-28, 3-31/3-32 thru 3-33/3-34 3-45/3-46, 4-1/4-2, 4-3/4-4 thru 4-13/4-14, 4-15/4-16, 4-19/4-20, 4-23/4-24 thru 4-29/4-30, 4-33/4-34, 4-37/4-38, 4-39/4-39.a and 4-39.b/4-40, 4-41/4-42, 5-1/5-2 thru 5-3/5-4, 5-9/5-10 thru 5-11/5-12, 5-17/5-18, 5-25/5-26, 6-1/6-2 thru 6-3/6-4, 6-9/6-10 thru 6-17/6-18, 6-23/6-24 thru 6-25/6-26, IN-1/IN-2 thru IN-15/IN-16	4-2.a/4-2.b, 4-14.a/4-14.b, 4-16.a/4-16.b, 4-38.a/4-38.b,

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- ❑ The supplement number is shown at the bottom of each replacement page.

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Preface

This manual will provide board level information, and detailed ASIC chip information including register bit descriptions for the MVME197 series of Single Board Computers.

This manual is intended for anyone who wants to program these boards in order to design OEM systems, supply additional capability to an existing compatible system, or work in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* section found in the following pages.

Manual Terminology

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format, as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

For example, "12" is the decimal number twelve, and "$12" is the decimal number eighteen. Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

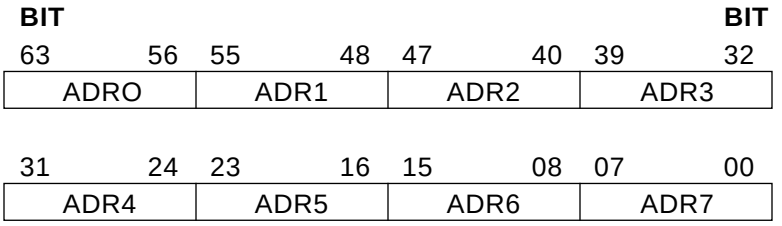
An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

- A *byte* is eight bits, numbered 0 through 7, with bit 0 being the least significant.
- A two-byte is 16 bits, numbered 0 through 15, with bit 0 being the least significant. For the MVME197 and other RISC modules, this is called a *half-word*.
- A four-byte is 32 bits, numbered 0 through 31, with bit 0 being the least significant. For the MVME197 and other RISC modules, this is called a *word*.
- An eight-byte is 64 bits, numbered 0 through 63, with bit 0 being the least significant. For the MVME197 and other RISC modules, this is called a *double-word*.

Throughout this manual, it is assumed that the MPU on the MVME197 module series is always programmed with *big-endian byte ordering*, as shown below. Any attempt to use *small-endian byte ordering* will immediately render the MVME197Bug debugger unusable.



The terms control bit and status bit are used extensively in this document. The term control bit is used to describe a bit in a register that can be set and cleared under software control. The term true is used to indicate that a bit is in the state that enables the function it controls. The term false is used to indicate that the bit is in the state that disables the function it controls. In all tables, the terms 0 and 1 are used to describe the actual value that should be written to the bit, or the value that it yields when read. The term status bit is used to describe a bit in a register that reflects a specific condition. The status bit can be read by software to determine operational or exception conditions.

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BOARD LEVEL HARDWARE DESCRIPTION 1

Introduction

This manual provides programming information for the MVME197 series of Single Board Computers. Extensive programming information is provided for the Application-Specific Integrated Circuit (ASIC) devices used on the MVME197 module series. Refer to the next section for model designations.

This chapter describes the board level hardware features of the MVME197 series of single board computers, hereafter referred to as the MVME197, unless separately specified. The chapter is organized with a board level overview and features listed in this introduction, followed by a more detailed hardware functional description. Front panel switches and indicators are included in the detailed hardware functional description. Memory maps are next, and the chapter closes with some general software considerations.

All programmable registers in the MVME197 reside in ASICs and are covered in device specific chapters. Chapter 2 covers the VMEchip2 (VME2), Chapter 3 covers the PCCchip2 (PCC2), Chapter 4 covers the BusSwitch gate array, Chapter 5 covers the DCAM (DRAM Controller and Address Multiplexer), and Chapter 6 covers the ECDM (Error Correction and Data Multiplexer). For those interested in programmable register bit definitions and less interested in hardware functionality, focus on Chapters 2, 3, 4, 5, and 6. In some cases, however, Chapter 1 gives related background information.

Model Designations

The MVME197 Single Board Computer is available in the following models.

MVME197 Model Designations

Model Number	Motorola Part Number	Model Description
MVME197LE series		
MVME197-001	01-W3869B03L	Single Processor MC88110, 32MB Onboard ECC DRAM, 50 MHz
MVME197-002	01-W3869B04L	Single Processor MC88110, 64MB Onboard ECC DRAM, 50 MHz

MVME197 Model Designations (Continued)

Model Number	Motorola Part Number	Model Description
MVME197LE series		
MVME197-003	01-W3869B01M	Single Processor MC88110, 32MB Onboard ECC DRAM, 40 MHz
MVME197-004	01-W3869B02M	Single Processor MC88110, 64MB Onboard ECC DRAM, 40 MHz
MVME197SP series		
MVME197-101	01-W3815B02	Single Processor MC88110, 256KB Cache, 128MB Onboard ECC DRAM, 50 MHz
MVME197DP series		
MVME197-201	01-W3815B01	Dual Processor MC88110, 256KB Cache per Processor, 128MB Onboard ECC DRAM, 50 MHz
MVME197-202	01-W3815B03	Dual Processor MC88110, 256KB Cache per Processor, 256MB Onboard ECC DRAM, 50 MHz

Overview

Each MVME197 module is a double-high VMEmodule based on the MC88110 RISC microprocessor.

The **MVME197LE** series have 32/64MB of DRAM, 1MB of flash memory, 8KB of static RAM (with battery backup), a time of day clock (with battery backup), an Ethernet transceiver interface, four serial ports with EIA-232-D interface, six tick timers, a watchdog timer, 128/256KB of BOOT ROM, a SCSI bus interface with DMA (Direct Memory Access), a Centronics printer port, an A16/A24/A32/D8/D16/D32 VMEbus master/slave interface, and a VMEbus system controller.

The **MVME197DP/SP** series have 128/256MB of DRAM, 256KB of cache memory for **each** MC88110/MC88410 microprocessor/cache controller combination (note that the MVME197SP version has only one MC88110/MC88410 device combination), 1MB of flash memory, 8KB of static RAM (with battery backup), a time of day clock (with battery backup), an Ethernet transceiver interface, four serial ports with EIA-232-D interface, six tick timers,

a watchdog timer, 128/256KB of BOOT ROM, a SCSI bus interface with DMA (Direct Memory Access), a Centronics printer port, an A16/A24/A32/D8/D16/D32 VMEbus master/slave interface, and a VMEbus system controller.

Input/Output (I/O) signals are routed through the MVME197's backplane connector P2. A P2 Adapter Board or LCP2 Adapter board routes the signals and grounds from connector P2 to an MVME712 series transition module. The MVME197 supports the MVME712M, MVME712A, MVME712AM, and MVME712B transition boards (referred to here as the MVME712X, unless separately specified). The MVME197 also supports the MVME712-12 and MVME712-13 (referred to as the MVME712-XX, unless separately specified). These transition boards provide configuration headers, serial port drivers, and industry standard connectors for the I/O devices.

All MVME197 modules have eight ASICs (described in the following order: BusSwitch, DCAM, ECDM, PCC2, and VME2).

Note **For the MVME197 series, the term Local Bus, as used in other MVME1xx Single Board Computer series, is referred to as the Local Peripheral Bus.**

The BusSwitch ASIC provides an interface between the processor bus (MC88110 bus) and the local peripheral bus (MC68040 compatible bus). Refer to the board specific MVME197 block diagram (Figures 1-1, 1-2, and 1-3). It provides bus arbitration for the MC88110 bus and serves as a seven level interrupt handler. It has programmable map decoders for both busses, as well as write post buffers on each, two tick timers, and four 32-bit general purpose registers.

The DCAM (DRAM Controller and Address Multiplexer) ASIC provides the address multiplexers and RAS/CAS/WRITE control for the DRAM as well as data control for the ECDM.

The ECDM (Error Correction and Data Multiplexer) ASIC multiplexes between four data paths on the DRAM array. Since the device handles 16 bits, four such devices are required on the MVME197 to accommodate the 64-bit data bus of the MC88110 microprocessor. Single-bit error correction and double-bit detection is performed in the ECDM.

The PCCchip2 (Peripheral Channel Controller) ASIC provides two tick timers and the interface to the LAN chip, the SCSI chip, the serial port chip, the printer port, and the BBRAM (Battery Backup RAM).

The VMEchip2 ASIC provides a VMEbus interface. The VMEchip2 includes two tick timers, a watchdog timer, programmable map decoders for the master and slave interfaces, and a VMEbus to/from the local peripheral bus DMA controller, a VMEbus to/from the local peripheral bus non-DMA programmed access interface, a VMEbus interrupter, a VMEbus system controller, a VMEbus interrupt handler, and a VMEbus requester.

Local peripheral bus to VMEbus transfers can be D8, D16, or D32. VMEchip2 DMA transfers to the VMEbus, however, can be 64 bits wide as Block Transfer (BLT).

Requirements

These boards are designed to conform to the requirements of the following documents:

- ❏ VMEbus Specification (IEEE 1014-87)
- ❏ EIA-232-D Serial Interface Specification, EIA
- ❏ SCSI Specification, ANSI

Features

These are some of the major features of the MVME197 module series:

- ❏ Single MC88110 RISC Microprocessor (MVME197LE module series)
- ❏ Single MC88110 RISC Microprocessor with an MC88410 Cache Controller (MVME197SP module series)
- ❏ Dual MC88110 RISC Microprocessors, each with one MC88410 Cache Controller (MVME197DP module series)
- ❏ 256 kilobytes of external cache per processor, controlled by the MC88410 (MVME197DP and MVME197SP module series)
- ❏ 32 or 64 megabytes of 64-bit Dynamic Random Access Memory (DRAM) with Error Checking and Correction (ECC) (MVME197LE module series)
- ❏ 128 or 256 megabytes of 64-bit Dynamic Random Access Memory (DRAM) with Error Checking and Correction (ECC) (MVME197DP/SP module series)
- ❏ 1 megabyte of Flash memory
- ❏ Six status LEDs (FAIL, RUN, SCON, LAN, SCSI, and VME)
- ❏ 8 kilobytes of Static Random Access Memory (SRAM) and Time of Day (TOD) clock with battery backup RAM (BBRAM)
- ❏ Two push-button switches (ABORT and RESET)
- ❏ 128 or 256 kilobytes of BOOT ROM
- ❏ Six 32-bit tick timers for periodic interrupts
- ❏ Watchdog timer
- ❏ Eight software interrupts
- ❏ I/O
  - – SCSI Bus interface with Direct Memory Access (DMA)
  - – Four serial ports with EIA-232-D buffers

- Centronics printer port
- Ethernet transceiver interface

❑ VMEbus interface

- VMEbus system controller functions
- VMEbus interface to local peripheral bus (A24/A32, D8/D16/D32 BLT (D8/D16/D32/D64))(BLT = Block Transfer)
- Local peripheral bus to VMEbus interface (A24/A32, D8/D16/D32 BLT (D16/D32/D64))
- VMEbus interrupter
- VMEbus interrupt handler
- Global CSR for inter-processor communications
- DMA for fast local memory - VMEbus transfers (A16/A24/A32, D16/D32 BLT (D16/D32/D64))

Block Diagrams

General block diagrams for the MVME197 series of single board computers are provided as follows. Figure 1-1 illustrates the block diagram for the MVME197LE, Figure 1-2 illustrates the block diagram for the MVME197SP, and Figure 1-3 illustrates the block diagram for the MVME197DP.

Functional Description

This section contains a functional description of the major blocks on the MVME197 series of single board computers.

Front Panel Switches and Indicators

There are two push-button switches and six LEDs on the front panel of the MVME197. The switches are RESET and ABORT. The RESET switch (S3) will reset all onboard devices and drive the SYSRESET* signal if the board **is** the system controller. The RESET switch (S3) will reset all onboard devices except the DCAM and ECDM if the board **is not** the system controller. The VMEchip2 generates the SYSRESET* signal. The BusSwitch combines the VMEchip2 local reset, the power up reset, and the reset switch to generate a local board reset. Refer to the *Reset Module* section in the *BusSwitch* chapter for more information.

The ABORT switch (S2) can generate an interrupt to CPU0 via the NMI* signal. It is normally used to abort program execution and return to the debugger. This capability is controlled via the ABORT register in the BusSwitch.

The six LEDs on the MVME197 front panel are: FAIL, SCON, RUN, LAN, VME, and SCSI.

The yellow FAIL LED (DS1) is lit when the BRDFAIL signal line is active.

The green SCON LED (DS2) is lit when the VMEchip2 is the VMEbus system controller.

The green RUN LED (DS3) is lit when the MC88110 bus MC* pin is low.

The green LAN LED (DS4) lights when the LAN chip is the local peripheral bus master.

The green VME LED (DS5) lights when the board is using the VMEbus or when the board is accessed by the VMEbus.

The green SCSI LED (DS6) lights when the SCSI chip is the local peripheral bus master.

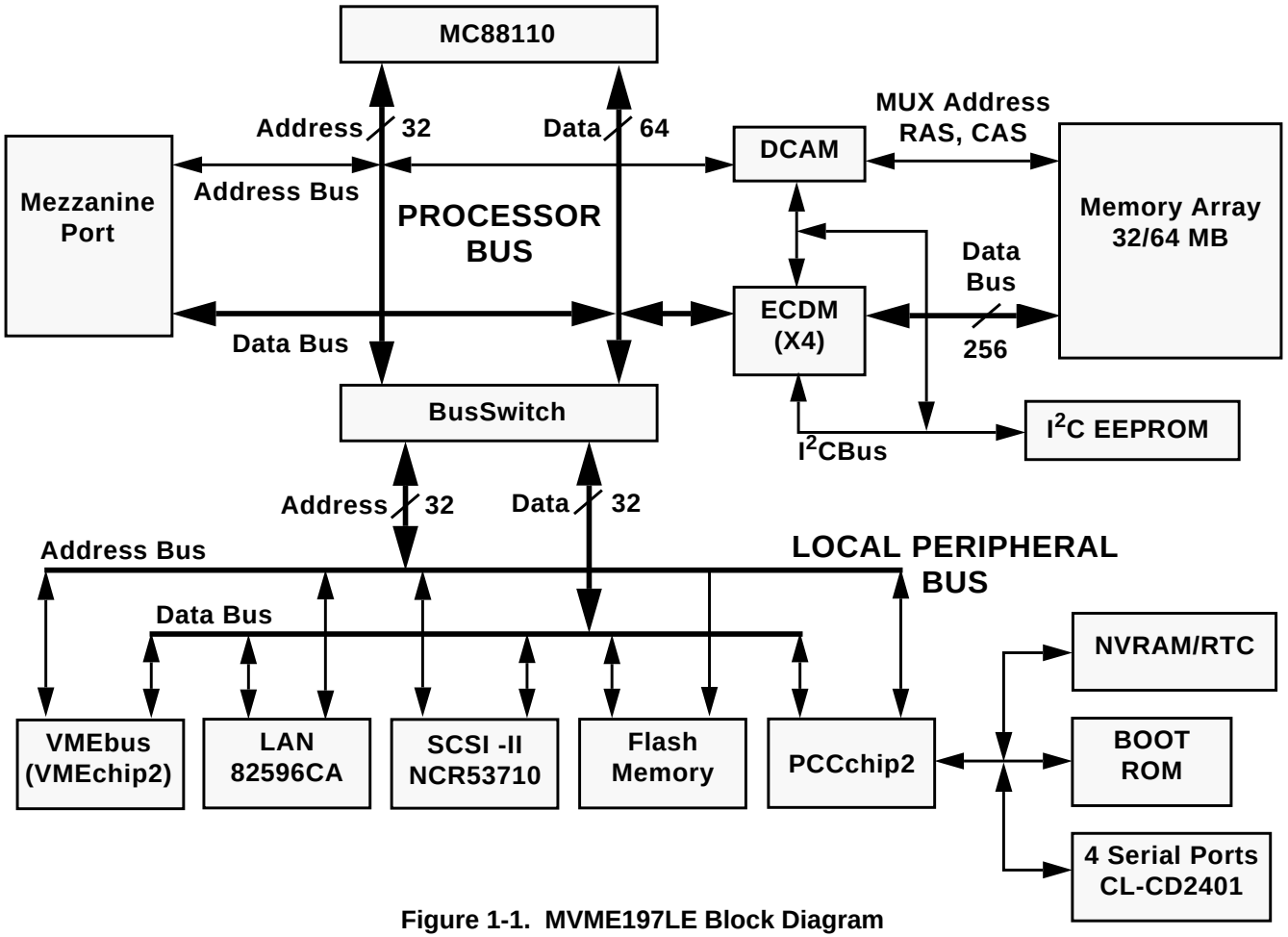

Figure 1-1. MVME197LE Block Diagram