

Supplement to
MVME197LE, MVME197DP, and MVME197SP
Single Board Computers
Programmer's Reference Guide
(MVME197PG/D1)

The attached pages are replacements for the corresponding pages in the manual. Place this page behind the title page of the manual as a record of this change. Please replace the pages according to the following table:

Replace Old	With New	Add New
iii/iv, ix/x thru xxiii/xxiv 1-1/1-2, 1/3-1-4, 1-5/1-6, 1-7/1-8, 1-13/1-14, 1-15/1-16 thru 1-25/1-26, 2-1/2-2 thru 2-3/2-4, 2-17/2-18 thru 2-19/2-20, 2-25/2-26 thru 2-27/2-28, 2-31/2-32 thru 2-37/2-38, 2-41/2-42 thru 2-45/2-46, 2-49/2-50, 2-53/2-54, 2-63/2-64 thru 2-65/2-66, 2-89/2-90 thru 2-91/2-92, 2-95/2-96	iii/iv, ix/x thru xxiii/xxiv 1-1/1-1.a and 1-1.b/1-2, 1-3/1-3.a and 1-3.b/1-4, 1-5/1-5.a and 1-5.b/1-6, 1-7/1-8, 1-13/1-13a and 1-13.b/1-14, 1-15/1-16 thru 1-25/1-26, 2-1/2-2 thru 2-3/2-4, 2-17/2-18 thru 2-19/2-20, 2-25/2-26 thru 2-27/2-28, 2-31/2-32 thru 2-37/2-38, 2-41/2-42 thru 2-45/2-46, 2-49/2-50, 2-53/2-54, 2-63/2-64 thru 2-65/2-66, 2-89/2-90 thru 2-91/2-92, 2-95/2-96	1-6.a/1-6.b,

Replace Old	With New	Add New
3-1/3-2, 3-3/3-4, 3-7/3-8 thru 3-9/3-10, 3-13/3-14, 3-17/3-18 thru 3-19/3-20, 3-27/3-28, 3-31/3-32 thru 3-33/3-34 3-45/3-46, 4-1/4-2, 4-3/4-4 thru 4-13/4-14, 4-15/4-16, 4-19/4-20, 4-23/4-24 thru 4-29/4-30, 4-33/4-34, 4-37/4-38, 4-39/4-40, 4-41/4-42, 5-1/5-2 thru 5-3/5-4, 5-9/5-10 thru 5-11/5-12, 5-17/5-18, 5-25/5-26, 6-1/6-2 thru 6-3/6-4, 6-9/6-10 thru 6-17/6-18, 6-23/6-24 thru 6-25/6-26, IN-1/IN-2 thru IN-15/IN-16	3-1/3-2, 3-3/3-3.a and 3-3.b/3-4, 3-7/3-8 thru 3-9/3-10, 3-13/3-14, 3-17/3-18 thru 3-19/3-20, 3-27/3-28, 3-31/3-32 thru 3-33/3-34 3-45/3-46, 4-1/4-2, 4-3/4-4 thru 4-13/4-14, 4-15/4-16, 4-19/4-20, 4-23/4-24 thru 4-29/4-30, 4-33/4-34, 4-37/4-38, 4-39/4-39.a and 4-39.b/4-40, 4-41/4-42, 5-1/5-2 thru 5-3/5-4, 5-9/5-10 thru 5-11/5-12, 5-17/5-18, 5-25/5-26, 6-1/6-2 thru 6-3/6-4, 6-9/6-10 thru 6-17/6-18, 6-23/6-24 thru 6-25/6-26, IN-1/IN-2 thru IN-15/IN-16	4-2.a/4-2.b, 4-14.a/4-14.b, 4-16.a/4-16.b, 4-38.a/4-38.b,

- ❑ A vertical bar (|) in the margin of a replacement page indicates a text change or addition.
- ❑ The supplement number is shown at the bottom of each replacement page.

Notice

While reasonable efforts have been made to assure the accuracy of this document, Motorola, Inc. assumes no liability resulting from any omissions in this document, or from the use of the information obtained therein. Motorola reserves the right to revise this document and to make changes from time to time in the content hereof without obligation of Motorola to notify any person of such revision or changes.

No part of this material may be reproduced or copied in any tangible medium, or stored in a retrieval system, or transmitted in any form, or by any means, radio, electronic, mechanical, photocopying, recording or facsimile, or otherwise, without the prior written permission of Motorola, Inc.

Restricted Rights Legend

If the documentation contained herein is supplied, directly or indirectly, to the U.S. Government, the following notice shall apply unless otherwise agreed to in writing by Motorola, Inc.

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subparagraph (c)(1)(ii) of the Rights in Technical Data and Computer Software clause at DFARS 252.227-7013.

Motorola, Inc.
Computer Group
2900 South Diablo Way
Tempe, Arizona 85282-9602

Preface

This manual will provide board level information, and detailed ASIC chip information including register bit descriptions for the MVME197 series of Single Board Computers.

This manual is intended for anyone who wants to program these boards in order to design OEM systems, supply additional capability to an existing compatible system, or work in a lab environment for experimental purposes.

A basic knowledge of computers and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* section found in the following pages.

Manual Terminology

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format, as follows:

\$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

For example, "12" is the decimal number twelve, and "\$12" is the decimal number eighteen. Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, *assertion* and *negation* are used to specify forcing a signal to a particular state. In particular, *assertion* and *assert* refer to a signal that is active or true; *negation* and *negate* indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

- ❑ A *byte* is eight bits, numbered 0 through 7, with bit 0 being the least significant.
- ❑ A two-byte is 16 bits, numbered 0 through 15, with bit 0 being the least significant. For the MVME197 and other RISC modules, this is called a *half-word*.
- ❑ A four-byte is 32 bits, numbered 0 through 31, with bit 0 being the least significant. For the MVME197 and other RISC modules, this is called a *word*.
- ❑ An eight-byte is 64 bits, numbered 0 through 63, with bit 0 being the least significant. For the MVME197 and other RISC modules, this is called a *double-word*.

Throughout this manual, it is assumed that the MPU on the MVME197 module series is always programmed with *big-endian byte ordering*, as shown below. Any attempt to use *small-endian byte ordering* will immediately render the MVME197Bug debugger unusable.

BIT	63	56	55	48	47	40	39	BIT
	ADRO		ADR1		ADR2		ADR3	
	31	24	23	16	15	08	07	00
	ADR4		ADR5		ADR6		ADR7	

The terms control bit and status bit are used extensively in this document. The term control bit is used to describe a bit in a register that can be set and cleared under software control. The term true is used to indicate that a bit is in the state that enables the function it controls. The term false is used to indicate that the bit is in the state that disables the function it controls. In all tables, the terms 0 and 1 are used to describe the actual value that should be written to the bit, or the value that it yields when read. The term status bit is used to describe a bit in a register that reflects a specific condition. The status bit can be read by software to determine operational or exception conditions.

Contents

CHAPTER 1 BOARD LEVEL HARDWARE DESCRIPTION

Introduction	1-1
Model Designations	1-1
Overview	1-1.a
Requirements	1-3
Features.....	1-3
Block Diagram	1-4
Functional Description	1-4
Front Panel Switches and Indicators.....	1-4
Data Bus Structure	1-6
MC88110 MPU.....	1-6
MC88410 Cache Controller.....	1-6
BOOT ROM.....	1-6
Flash Memory.....	1-6
Onboard DRAM.....	1-6.a
Battery Backup RAM and Clock.....	1-7
VMEbus Interface	1-7
I/O Interfaces	1-7
Serial Port Interface	1-7
Printer Interface	1-8
Ethernet Interface.....	1-8
SCSI Interface	1-9
SCSI Termination.....	1-9
Peripheral Resources	1-9
Programmable Tick Timers.....	1-9
Watchdog Timer	1-10
Software-Programmable Hardware Interrupts.....	1-10
Processor Bus Timeout.....	1-10
Local Peripheral Bus Timeout.....	1-10
Interrupt Sources.....	1-10
Configuration Switches.....	1-11
Configuration Switch S1: General Information.....	1-11
Configuration Switch S1: General Purpose Functions (S1-1 to S1-8).....	1-12
Configuration Switch S1: System Controller Enable Function (S1-9).....	1-12

Configuration Switch S6: Serial Port 4 Clock Select (S6-1, S6-2).....	1-13
Connectors	1-13
Memory Maps	1-14
Processor Bus Memory Map	1-14
Detailed I/O Memory Maps.....	1-17
BBRAM, TOD Clock Memory Map	1-30
VMEbus Memory Map	1-32
VMEbus Accesses to the Local Peripheral Bus	1-32
VMEbus Short I/O Memory Map.....	1-32
Software Support Considerations	1-32

CHAPTER 2 VMEchip2

Introduction	2-1
VMEchip2 Features	2-1
Functional Description.....	2-3
Local Peripheral Bus to VMEbus Interface	2-5
Local Peripheral Bus to VMEbus Requester.....	2-7
VMEbus to Local Peripheral Bus Interface	2-8
Local Peripheral Bus to VMEbus DMA Controller	2-9
DMAC VMEbus Requester	2-11
Tick and Watchdog Timers.....	2-12
Prescaler.....	2-12
Tick Timer.....	2-12
Watchdog Timer	2-13
VMEbus Interrupter	2-13
VMEbus System Controller.....	2-14
Arbiter	2-14
IACK Daisy-Chain Driver.....	2-14
Bus Timer.....	2-14
Reset Driver.....	2-15
Local Peripheral Bus Interrupter and Interrupt Handler	2-15
Global Control and Status Registers	2-16
VMEboard Functions	2-17
LCSR Programming Model	2-17
Programming the VMEbus Slave Map Decoders	2-21
VMEbus Slave Ending Address Register 1.....	2-22
VMEbus Slave Starting Address Register 1.....	2-23
VMEbus Slave Ending Address Register 2.....	2-23
VMEbus Slave Starting Address Register 2.....	2-23

VMEbus Slave Address Translation Address Register 1	2-24
VMEbus Slave Address Translation Select Register 1	2-24
VMEbus Slave Address Translation Address Register 2	2-24
VMEbus Slave Address Translation Select Register 2	2-25
VMEbus Slave Write Post and Snoop Control Register 2	2-25
VMEbus Slave Address Modifier Select Register 2	2-26
VMEbus Slave Write Post and Snoop Control Register 1	2-27
VMEbus Slave Address Modifier Select Register 1	2-28
Programming the Local Peripheral Bus to VMEbus Map Decoders	2-29
Local Peripheral Bus Slave Ending Address Register 1	2-31
Local Peripheral Bus Slave Starting Address Register 1	2-31
Local Peripheral Bus Slave Ending Address Register 2	2-31
Local Peripheral Bus Slave Starting Address Register 2	2-32
Local Peripheral Bus Slave Ending Address Register 3	2-32
Local Peripheral Bus Slave Starting Address Register 3	2-32
Local Peripheral Bus Slave Ending Address Register 4	2-33
Local Peripheral Bus Slave Starting Address Register 4	2-33
Local Peripheral Bus Slave Address Translation	
Address Register 4	2-33
Local Peripheral Bus Slave Address Translation Select	
Register 4	2-34
Local Peripheral Bus Slave Attribute Register 4	2-34
Local Peripheral Bus Slave Attribute Register 3	2-35
Local Peripheral Bus Slave Attribute Register 2	2-36
Local Peripheral Bus Slave Attribute Register 1	2-37
VMEbus Slave GCSR Group Address Register	2-38
VMEbus Slave GCSR Board Address Register	2-39
Local Peripheral Bus to VMEbus Enable Control Register	2-40
Local Peripheral Bus to VMEbus I/O Control Register	2-41
ROM Control Register	2-42
Programming the VMEchip2 DMA Controller	2-42
DMAC Registers	2-43
EPROM Decoder, SRAM and DMA Control Register	2-44
Local Peripheral Bus to VMEbus Requester Control Register	2-46
DMAC Control Register 1 (bits 0-7)	2-47
DMAC Control Register 2 (bits 8-15)	2-48
DMAC Control Register 2 (bits 0-7)	2-50
DMAC Local Peripheral Bus Address Counter Register	2-51
DMAC VMEbus Address Counter Register	2-51
DMAC Byte Counter Register	2-52
Table Address Counter Register	2-52
VMEbus Interrupter Control Register	2-53

VMEbus Interrupter Vector Register.....	2-54
MPU Status and DMAC Interrupt Count Register	2-54
DMAC Status Register.....	2-55
Programming the Tick and Watchdog Timers.....	2-56
VMEbus Arbiter Timeout Control Register	2-56
DMAC Ton/Toff Timers and VMEbus Global Timeout Control Register	2-57
VME Access, Local Peripheral Bus and Watchdog Timeout Control Register	2-58
Prescaler Control Register.....	2-60
Tick Timer 1 Compare Register.....	2-61
Tick Timer 1 Counter Register.....	2-61
Tick Timer 2 Compare Register.....	2-62
Tick Timer 2 Counter Register.....	2-62
Board Control Register	2-63
Watchdog Timer Control Register.....	2-64
Tick Timer 2 Control Register	2-65
Tick Timer 1 Control Register	2-66
Prescaler Counter Register.....	2-66
Programming the Local Peripheral Bus Interrupter.....	2-67
Local Peripheral Bus Interrupter Status Register (bits 24-31).....	2-69
Local Peripheral Bus Interrupter Status Register (bits 16-23).....	2-70
Local Peripheral Bus Interrupter Status Register (bits 8-15).....	2-71
Local Peripheral Bus Interrupter Status Register (bits 0-7).....	2-72
Local Peripheral Bus Interrupter Enable Register (bits 24-31).....	2-73
Local Peripheral Bus Interrupter Enable Register (bits 16-23).....	2-74
Local Peripheral Bus Interrupter Enable Register (bits 8-15).....	2-75
Local Peripheral Bus Interrupter Enable Register (bits 0-7).....	2-76
Software Interrupt Set Register (bits 8-15).....	2-77
Interrupt Clear Register (bits 24-31)	2-78
Interrupt Clear Register (bits 16-23)	2-79
Interrupt Clear Register (bits 8-15)	2-80
Interrupt Level Register 1 (bits 24-31)	2-81
Interrupt Level Register 1 (bits 16-23)	2-81
Interrupt Level Register 1 (bits 8-15)	2-82
Interrupt Level Register 1 (bits 0-7)	2-82
Interrupt Level Register 2 (bits 24-31)	2-83
Interrupt Level Register 2 (bits 16-23)	2-83
Interrupt Level Register 2 (bits 8-15)	2-84
Interrupt Level Register 2 (bits 0-7)	2-84
Interrupt Level Register 3 (bits 24-31)	2-85
Interrupt Level Register 3 (bits 16-23)	2-85

Interrupt Level Register 3 (bits 8-15)	2-86
Interrupt Level Register 3 (bits 0-7)	2-86
Interrupt Level Register 4 (bits 24-31)	2-87
Interrupt Level Register 4 (bits 16-23)	2-87
Interrupt Level Register 4 (bits 8-15)	2-88
Interrupt Level Register 4 (bits 0-7)	2-88
Vector Base Register	2-89
I/O Control Register 1	2-90
I/O Control Register 2	2-91
I/O Control Register 3	2-92
GCSR Programming Model.....	2-94
Programming the GCSR	2-95
VMEchip2 Revision Register.....	2-97
VMEchip2 ID Register	2-97
VMEchip2 LM/SIGI Register.....	2-97
VMEchip2 Board Status/Control Register	2-99
General Purpose Control and Status Register 0.....	2-100
General Purpose Control and Status Register 1.....	2-100
General Purpose Control and Status Register 2.....	2-100
General Purpose Control and Status Register 3.....	2-101
General Purpose Control and Status Register 4.....	2-101
General Purpose Control and Status Register 5.....	2-101

CHAPTER 3 PCCchip2

Introduction	3-1
PCCchip2 Features.....	3-1
Functional Description	3-1
General Description.....	3-1
BBRAM Interface	3-3
Download ROM Interface.....	3-3
82596CA LAN Controller Interface.....	3-3
MPU Port and MPU Channel Attention	3-3
MC68040 Bus Master Support for 82596CA	3-4
LANC Bus Error.....	3-4
LANC Interrupt	3-5
53C710 SCSI Controller Interface.....	3-5
Memory Controller MEMC040 Interface.....	3-5
Parallel Port Interface.....	3-5
General Purpose I/O Pin.....	3-6
CD2401 SCC Interface	3-6

Interrupt Prioritizer.....	3-8
Tick Timer	3-8
Overall Memory Map.....	3-8
CSR Programming Model	3-9
Chip ID Register	3-11
Chip Revision Register	3-11
General Control Register.....	3-12
Vector Base Register.....	3-13
Programming the Tick Timers	3-14
Tick Timer 1 Compare Register.....	3-14
Tick Timer 1 Counter Register.....	3-15
Tick Timer 2 Compare Register.....	3-15
Tick Timer 2 Counter Register.....	3-16
Prescaler Count Register	3-16
Prescaler Clock Adjust Register	3-17
Tick Timer 2 Control Register	3-18
Tick Timer 1 Control Register	3-19
General Purpose Input Interrupt Control Register	3-20
General Purpose Input/Output Pin Control Register	3-21
Tick Timer 2 Interrupt Control Register	3-22
Tick Timer 1 Interrupt Control Register	3-23
SCC Error Status Register and Interrupt Control Registers	3-24
SCC Error Status Register	3-24
SCC Modem Interrupt Control Register	3-25
SCC Transmit Interrupt Control Register.....	3-26
SCC Receive Interrupt Control Register	3-27
Modem PIACK Register.....	3-28
Transmit PIACK Register.....	3-29
Receive PIACK Register	3-30
LANC Error Status and Interrupt Control Registers.....	3-31
LANC Error Status Register	3-31
82596CA LANC Interrupt Control Register	3-32
LANC Bus Error Interrupt Control Register.....	3-33
Programming the SCSI Error Status and Interrupt Registers	3-34
SCSI Error Status Register.....	3-34
SCSI Interrupt Control Register	3-35
Programming the Printer Port.....	3-36
Printer ACK Interrupt Control Register	3-36
Printer FAULT Interrupt Control Register	3-37
Printer SEL Interrupt Control Register	3-38
Printer PE Interrupt Control Register	3-39
Printer BUSY Interrupt Control Register	3-40

Printer Input Status Register.....	3-41
Printer Port Control Register	3-42
Chip Speed Register	3-43
Printer Data Register	3-44
Interrupt Priority Level Register	3-45
Interrupt Mask Level Register	3-46

CHAPTER 4 BUSSWITCH

Introduction	4-1
BusSwitch Features.....	4-1
System Overview	4-1
Processor Bus Functions.....	4-3
Processor Bus Arbiter	4-3
Processor Bus Decoder	4-3
Processor Write Post Buffer	4-4
Processor Bus Timer	4-5
Processor Interrupter.....	4-5
INT* Interrupts.....	4-5
NMI* Interrupts.....	4-5
Reset Module.....	4-5
Local Peripheral Bus Functions.....	4-6
System Bus Requester	4-6
System Bus Timer.....	4-6
System Bus Map Decoder	4-6
Interrupt Handler	4-7
MC88410 Flush/Invalidate Control	4-7
BusSwitch Registers.....	4-7
Conventions	4-7
Chip ID Register - CHIPID.....	4-9
Chip Revision Register - CHIPREV	4-9
General Control and Status Register - GCSR.....	4-10
I/O Data Register - IODATA.....	4-12
I/O Direction Register - IODIR	4-13
Processor Start Address Register - PSAR(1-4).....	4-14
Processor End Address Register - PEAR(1-4).....	4-14.a
Processor Translation Register - PTR(1-4).....	4-15
Processor Translation Select Register - PTRS(1-4)	4-15
System Start Address Register - SSAR(1-4)	4-16
System End Address Register - SEAR(1-4)	4-16.a
System Translation Register - STR(1-4)	4-17

System Translation Select Register - STSR(1-4).....	4-17
Processor Attribute Register - PAR(1-4)	4-18
System Attribute Register - SAR(1-4)	4-19
Bus Timer Register - BTIMER.....	4-20
Prescaler Adjust Register - PADJUST	4-21
Prescaler Count Register - PCOUNT.....	4-21
Processor Address Log Register - PAL	4-22
Write Post Processor Address Register - WPPA.....	4-22
Write Post Translated Processor Address Register - WPTPA	4-23
Write Post Processor Attributes Register - WPPAT	4-23
ROM Control Register - ROMCR.....	4-24
Timer Control 1 Register - TCTRL1	4-26
Timer Control 2 Register - TCTRL2	4-26
Interrupt Level Register - LEVEL	4-27
Interrupt Mask Register - MASK	4-27
Interrupt Select 0 Register - ISEL0	4-28
Interrupt Select 1 Register - ISEL1	4-28
Abort Control Register - ABORT	4-29
Cross Processor Interrupt Register - CPINT	4-29
Timer Interrupt 1 Register - TINT1.....	4-30
Timer Interrupt 2 Register - TINT2.....	4-31
Write Post Interrupt Control Register - WPINT	4-31
Processor Address Log Interrupt Register - PALINT	4-32
External Interrupt Register- XINT	4-33
Vector Base Register - VBASE	4-34
Timer Compare 1 Register - TCOMP1	4-35
Timer Counter 1 Register - TCOUNT1	4-35
Timer Compare 2 Register - TCOMP2	4-36
Timer Counter 2 Register - TCOUNT2	4-36
General Purpose Register - GPR(1-4)	4-37
External Cache TAGS Register - XCTAGS	4-38
External Cache Control Register - XCCR.....	4-38
Vector Registers - VECTOR(1-7)	4-39
External Cache Flush Register - XCFR	4-39.a
Bus Operation.....	4-40
Processor Slave Interface	4-41
Processor Master Interface	4-41
Dual Processor Registers	4-42

CHAPTER 5 DRAM CONTROLLER AND ADDRESS MULTIPLEXER (DCAM)

Introduction	5-1
DCAM Features.....	5-1
System Overview	5-1
DCAM Gate Array Functions.....	5-3
General Operation	5-3
Read Cycles.....	5-3
Cache Read Cycles.....	5-4
Normal (non-burst) Write Cycles	5-5
Burst Write Cycles.....	5-5
Functional Block Description	5-5
Processor Address Buffers.....	5-5
State Machine Registers	5-6
Cycle Decode	5-6
Address Decode	5-6
Timing State Machine.....	5-7
CAS Boundary Checker	5-7
CAS Latches and Counters.....	5-7
RAS Address Latches	5-8
Address Multiplexer.....	5-8
Cache Address TAGs and Comparators.....	5-8
Refresh Counters and Control	5-8
DRAM Interface	5-9
Processor/BusSwitch Interface.....	5-9
ECDM Interface.....	5-9
JTAG Test Interface	5-9
Scrubbing	5-9
DCAM Auto-Program.....	5-10
DCAM Software Programming	5-10
DCAM Programmable Registers	5-11
DCAM Register Set.....	5-13
User Operating Registers	5-17
ID Register	5-17
Version Register.....	5-17
RAM Start Address Register 1 - RSAR1 (SL25-31).....	5-18
Disable RAM Bit - DISRAM.....	5-18
RAM Start Address Register 2 - RSAR2 (SH25-31).....	5-19
Single Scrub Bit - SCRUB1TIME.....	5-19
Refresh Count Register - (REF0-11).....	5-20
Interrupt/TA Bit - INTRRUPT	5-21
Scrub Count Register - (SC2-32)	5-22

CSR Address Mapping Register - (CSR 4-31).....	5-23
DRAM Size and Type Setup Registers.....	5-24
Page Mode Bit - PGMODE.....	5-24
One Bank Bit	5-24
DRAM Size Register	5-25
Hardware Setup Registers.....	5-26
CAS Clock Select Bit - CASCLKSL	5-26
CAS Clock Bits - (CASCLK1-2)	5-26
Refresh Tail Register - (REFTAIL1-4).....	5-27
Kill Cache Bit.....	5-27
Read Tail Select Register - (RDTAIL1-5).....	5-27
Read Tail Clock Select Bit - RTCLKSL.....	5-28
Read Acknowledge Select Register - (READACK1-7).....	5-28
Split RAS Bit.....	5-29
Read Output Enable Select Register - (READOE1-6).....	5-29
Latch First Word in ECDM Clock Select Bit - FECCLKSL	5-30
Burst Read Output Enable End Time Select Register - (BREADOE1-6)	5-30
Precharge Clock Select Bit - PCGCLKSL	5-31
Precharge Register - (PCHG0-7).....	5-32
Latch Second Word in ECDM Register - (SLECDM2-5).....	5-32
Latch First Word in ECDM Register - (FLECDM1-4)	5-33
End RAM Output Enable Register - (ERAMOE1-6).....	5-33
RAM Output Enable Clock Select Bit - ROECLKSL.....	5-34
Read-Modify-Write (normal write) RAM Output Enable Register - (RMWRMOE1-6).....	5-34
CSR Tail Select Register - (CSRTAIL1-7)	5-35
Read-Modify-Write (normal write) ECDM Output Enable Register - (RMWOE1-5)	5-35
Burst Write Tail Register - (BWRTTL1-4)	5-36
Latch Second Word in ECDM Clock Select Bit - SECCLKSL.....	5-36
Read-Modify-Write (normal write) ECDM Output Enable Clock Select Bit - RMWOCKSL.....	5-36
Burst Write Time Select Register - (BWRITE1-5).....	5-37
Burst Write Time Clock Select Bit - WRCLKSEL.....	5-37
Read-Modify-Write Write Time Select Register - (RMW1-5).....	5-37
Read-Modify-Write (normal write) Tail Register - (RMWTAIL1-7)	5-38
Read-Modify-Write (normal write) Tail Clock Select Bit - RMWTLCSL	5-38
Cache Burst Read Output Enable Select Register - (CBRDOE1-3).....	5-39

Cache Read Output Enable Register - (CREADOE1-3).....	5-39
Burst Write Tail Clock Select Bit - BWRTCSL	5-40
Cache Burst Read Tail Register - (CBTAIL1-4).....	5-40
Cache Burst Read Tail Clock Select Bit - CBTLCKSL	5-40
Burst Read Tail Select Register - (BRDTAIL1-5)	5-41
Functional Controls.....	5-41
Sleep Mode Pin.....	5-41
External Refresh	5-41
Disable In/Disable Out.....	5-42

CHAPTER 6 ERROR CORRECTION AND DATA MULTIPLEXER (ECDM)

Introduction	6-1
Overview	6-1
ECDM Features	6-1
General Description.....	6-2
ECDM Block Diagram.....	6-3
ECDM Hamming Code.....	6-4
ECDM Error Logging	6-6
ECDM Syndrome Decode.....	6-6
ECDM Configuration in a 64-Bit System.....	6-8
ECDM I ² Cbus Programming Reference	6-9
ECDM/DCAM I ² Cbus Operation.....	6-10
ECDM Register Map in a 64-Bit System	6-16
ECDM Control and Status Registers	6-16
CSR Operation.....	6-16
Memory Control Register - MEMCON	6-18
ECDM ID Register - ECDMID	6-20
Syndrome Status Register - SYNSTAT	6-20
Error Type Status Register - ERSTAT	6-21
I ² C Control Register - I2CON	6-23
I ² C Status Register - I2STAT	6-24
I ² C Data Register - I2DATA	6-25
I ² C Address Register - I2ADDR	6-26

CHAPTER 7 PRINTER AND SERIAL PORT CONNECTIONS

Introduction	7-1
--------------------	-----

List of Figures

Figure 1-1. MVME197LE Block Diagram.....	1-5
Figure 1-2. MVME197SP Block Diagram.....	1-5.a
Figure 1-3. MVME197DP Block Diagram.....	1-5.b
Figure 2-1. VMEchip2 Block Diagram.....	2-4
Figure 3-1. PCCchip2 Block Diagram.....	3-2
Figure 4-1. Simplified MC88110 System Block Diagram.....	4-2
Figure 4-1a. BusSwitch Block Diagram.....	4-2.a
Figure 5-1. Simplified MVME197 Block Diagram	5-2
Figure 6-1. ECDM Block Diagram	6-4
Figure 6-2. ECDM Modified Hamming Code.....	6-5
Figure 6-3. ECDM Syndrome Decode.....	6-7
Figure 6-4. 64-Bit ECDM Memory Configuration	6-8
Figure 6-5. Memory Sub-System CSR Architecture	6-10
Figure 7-1. Printer Port with MVME712A.....	7-2
Figure 7-2. Printer Port with MVME712M	7-3
Figure 7-3. Serial Port 1 Configured as DCE.....	7-4
Figure 7-4. Serial Port 2 Configured as DCE.....	7-5
Figure 7-5. Serial Port 3 Configured as DCE.....	7-6
Figure 7-6. Serial Port 4 Configured as DCE.....	7-7
Figure 7-7. Serial Port 1 Configured as DTE	7-8
Figure 7-8. Serial Port 2 Configured as DTE	7-9
Figure 7-9. Serial Port 3 Configured as DTE	7-10
Figure 7-10. Serial Port 4 Configured as DTE	7-11
Figure 7-11. Serial Port 1 with MVME712A	7-12
Figure 7-12. Serial Port 2 with MVME712A	7-13
Figure 7-13. Serial Port 3 with MVME712A	7-14
Figure 7-14. Serial Port 4 with MVME712A	7-15

List of Tables

Table 1-1. Processor Bus Memory Map	1-15
Table 1-2. Local Devices Memory Map	1-16
Table 1-3. BusSwitch Register Memory Map	1-18
Table 1-4. ECDM CSR Register Memory Map	1-19
Table 1-5. DCAM (I ² C) Register Memory Map.....	1-20
Table 1-6. VMEchip2 Memory Map.....	1-21
Table 1-7. PCCchip2 Memory Map.....	1-25
Table 1-8. Printer Memory Map	1-26
Table 1-9. Cirrus Logic CD2401 Serial Port Memory Map	1-27
Table 1-10. 82596CA Ethernet LAN Memory Map.....	1-28
Table 1-11. 53C710 SCSI Memory Map	1-29
Table 1-12. MK48T08 BBRAM, TOD Clock Memory Map	1-29
Table 1-13. BBRAM Configuration Area Memory Map.....	1-30
Table 1-14. TOD Clock Memory Map.....	1-30
Table 2-1. VMEchip2 Memory Map - LCSR Summary.....	2-18
Table 2-2. DMAC Command Table Format.....	2-43
Table 2-3. Local Peripheral Bus Interrupter Summary	2-68
Table 2-4. VMEchip2 Memory Map - GCSR Summary	2-96
Table 3-1. PCCchip2 Memory Map - Control and Status Registers	3-10
Table 4-1. BusSwitch Register Memory Map	4-8
Table 4-2. MC88110 Transfer Code Translation.....	4-40
Table 4-3. MC68040 Transfer Modifier Translation	4-41
Table 5-1. DCAM Register Map	5-11
Table 5-2. DCAM Register Set: User Registers.....	5-13
Table 5-3. DCAM Register Set: DRAM Size and Type Registers.....	5-13
Table 5-4. DCAM Register Set: Hardware Setup Registers.....	5-14
Table 6-1. ECDM CSR Register Memory Map	6-17

BOARD LEVEL HARDWARE DESCRIPTION

1

Introduction

This manual provides programming information for the MVME197 series of Single Board Computers. Extensive programming information is provided for the Application-Specific Integrated Circuit (ASIC) devices used on the MVME197 module series. Refer to the next section for model designations.

This chapter describes the board level hardware features of the MVME197 series of single board computers, hereafter referred to as the MVME197, unless separately specified. The chapter is organized with a board level overview and features listed in this introduction, followed by a more detailed hardware functional description. Front panel switches and indicators are included in the detailed hardware functional description. Memory maps are next, and the chapter closes with some general software considerations.

All programmable registers in the MVME197 reside in ASICs and are covered in device specific chapters. Chapter 2 covers the VMEchip2 (VME2), Chapter 3 covers the PCCchip2 (PCC2), Chapter 4 covers the BusSwitch gate array, Chapter 5 covers the DCAM (DRAM Controller and Address Multiplexer), and Chapter 6 covers the ECDM (Error Correction and Data Multiplexer). For those interested in programmable register bit definitions and less interested in hardware functionality, focus on Chapters 2, 3, 4, 5, and 6. In some cases, however, Chapter 1 gives related background information.

Model Designations

The MVME197 Single Board Computer is available in the following models.

MVME197 Model Designations

Model Number	Motorola Part Number	Model Description
MVME197LE series		
MVME197-001	01-W3869B03L	Single Processor MC88110, 32MB Onboard ECC DRAM, 50 MHz
MVME197-002	01-W3869B04L	Single Processor MC88110, 64MB Onboard ECC DRAM, 50 MHz

MVME197 Model Designations (Continued)

Model Number	Motorola Part Number	Model Description
MVME197LE series		
MVME197-003	01-W3869B01M	Single Processor MC88110, 32MB Onboard ECC DRAM, 40 MHz
MVME197-004	01-W3869B02M	Single Processor MC88110, 64MB Onboard ECC DRAM, 40 MHz
MVME197SP series		
MVME197-101	01-W3815B02	Single Processor MC88110, 256KB Cache, 128MB Onboard ECC DRAM, 50 MHz
MVME197DP series		
MVME197-201	01-W3815B01	Dual Processor MC88110, 256KB Cache per Processor, 128MB Onboard ECC DRAM, 50 MHz
MVME197-202	01-W3815B03	Dual Processor MC88110, 256KB Cache per Processor, 256MB Onboard ECC DRAM, 50 MHz

Overview

Each MVME197 module is a double-high VME module based on the MC88110 RISC microprocessor.

The **MVME197LE** series have 32/64MB of DRAM, 1MB of flash memory, 8KB of static RAM (with battery backup), a time of day clock (with battery backup), an Ethernet transceiver interface, four serial ports with EIA-232-D interface, six tick timers, a watchdog timer, 128/256KB of BOOT ROM, a SCSI bus interface with DMA (Direct Memory Access), a Centronics printer port, an A16/A24/A32/D8/D16/D32 VMEbus master/slave interface, and a VMEbus system controller.

The **MVME197DP/SP** series have 128/256MB of DRAM, 256KB of cache memory for **each** MC88110/MC88410 microprocessor/cache controller combination (note that the MVME197SP version has only one MC88110/MC88410 device combination), 1MB of flash memory, 8KB of static RAM (with battery backup), a time of day clock (with battery backup), an Ethernet transceiver interface, four serial ports with EIA-232-D interface, six tick timers,

a watchdog timer, 128/256KB of BOOT ROM, a SCSI bus interface with DMA (Direct Memory Access), a Centronics printer port, an A16/A24/A32/D8/D16/D32 VMEbus master/slave interface, and a VMEbus system controller.

Input/Output (I/O) signals are routed through the MVME197's backplane connector P2. A P2 Adapter Board or LCP2 Adapter board routes the signals and grounds from connector P2 to an MVME712 series transition module. The MVME197 supports the MVME712M, MVME712A, MVME712AM, and MVME712B transition boards (referred to here as the MVME712X, unless separately specified). The MVME197 also supports the MVME712-12 and MVME712-13 (referred to as the MVME712-XX, unless separately specified). These transition boards provide configuration headers, serial port drivers, and industry standard connectors for the I/O devices.

All MVME197 modules have eight ASICs (described in the following order: BusSwitch, DCAM, ECDM, PCC2, and VME2).

Note For the MVME197 series, the term **Local Bus**, as used in other MVME1xx Single Board Computer series, is referred to as the **Local Peripheral Bus**.

The BusSwitch ASIC provides an interface between the processor bus (MC88110 bus) and the local peripheral bus (MC68040 compatible bus). Refer to the board specific MVME197 block diagram (Figures 1-1, 1-2, and 1-3). It provides bus arbitration for the MC88110 bus and serves as a seven level interrupt handler. It has programmable map decoders for both busses, as well as write post buffers on each, two tick timers, and four 32-bit general purpose registers.

The DCAM (DRAM Controller and Address Multiplexer) ASIC provides the address multiplexers and RAS/CAS/WRITE control for the DRAM as well as data control for the ECDM.

The ECDM (Error Correction and Data Multiplexer) ASIC multiplexes between four data paths on the DRAM array. Since the device handles 16 bits, four such devices are required on the MVME197 to accommodate the 64-bit data bus of the MC88110 microprocessor. Single-bit error correction and double-bit detection is performed in the ECDM.

The PCCchip2 (Peripheral Channel Controller) ASIC provides two tick timers and the interface to the LAN chip, the SCSI chip, the serial port chip, the printer port, and the BBRAM (Battery Backup RAM).

The VMEchip2 ASIC provides a VMEbus interface. The VMEchip2 includes two tick timers, a watchdog timer, programmable map decoders for the master and slave interfaces, and a VMEbus to/from the local peripheral bus DMA controller, a VMEbus to/from the local peripheral bus non-DMA programmed access interface, a VMEbus interrupter, a VMEbus system controller, a VMEbus interrupt handler, and a VMEbus requester.

Local peripheral bus to VMEbus transfers can be D8, D16, or D32. VMEchip2 DMA transfers to the VMEbus, however, can be 64 bits wide as Block Transfer (BLT).

Requirements

These boards are designed to conform to the requirements of the following documents:

- ❑ VMEbus Specification (IEEE 1014-87)
- ❑ EIA-232-D Serial Interface Specification, EIA
- ❑ SCSI Specification, ANSI

Features

These are some of the major features of the MVME197 module series:

- ❑ Single MC88110 RISC Microprocessor (MVME197LE module series)
- ❑ Single MC88110 RISC Microprocessor with an MC88410 Cache Controller (MVME197SP module series)
- ❑ Dual MC88110 RISC Microprocessors, each with one MC88410 Cache Controller (MVME197DP module series)
- ❑ 256 kilobytes of external cache per processor, controlled by the MC88410 (MVME197DP and MVME197SP module series)
- ❑ 32 or 64 megabytes of 64-bit Dynamic Random Access Memory (DRAM) with Error Checking and Correction (ECC) (MVME197LE module series)
- ❑ 128 or 256 megabytes of 64-bit Dynamic Random Access Memory (DRAM) with Error Checking and Correction (ECC) (MVME197DP/SP module series)
- ❑ 1 megabyte of Flash memory
- ❑ Six status LEDs (FAIL, RUN, SCON, LAN, SCSI, and VME)
- ❑ 8 kilobytes of Static Random Access Memory (SRAM) and Time of Day (TOD) clock with battery backup RAM (BBRAM)
- ❑ Two push-button switches (ABORT and RESET)
- ❑ 128 or 256 kilobytes of BOOT ROM
- ❑ Six 32-bit tick timers for periodic interrupts
- ❑ Watchdog timer
- ❑ Eight software interrupts
- ❑ I/O
 - SCSI Bus interface with Direct Memory Access (DMA)
 - Four serial ports with EIA-232-D buffers

- Centronics printer port
- Ethernet transceiver interface
- VMEbus interface
 - VMEbus system controller functions
 - VMEbus interface to local peripheral bus (A24/A32, D8/D16/D32 BLT (D8/D16/D32/D64))(BLT = Block Transfer)
 - Local peripheral bus to VMEbus interface (A24/A32, D8/D16/D32 BLT (D16/D32/D64))
 - VMEbus interrupter
 - VMEbus interrupt handler
 - Global CSR for inter-processor communications
 - DMA for fast local memory - VMEbus transfers (A16/A24/A32, D16/D32 BLT (D16/D32/D64))

Block Diagrams

General block diagrams for the MVME197 series of single board computers are provided as follows. Figure 1-1 illustrates the block diagram for the MVME197LE, Figure 1-2 illustrates the block diagram for the MVME197SP, and Figure 1-3 illustrates the block diagram for the MVME197DP.

Functional Description

This section contains a functional description of the major blocks on the MVME197 series of single board computers.

Front Panel Switches and Indicators

There are two push-button switches and six LEDs on the front panel of the MVME197. The switches are RESET and ABORT. The RESET switch (S3) will reset all onboard devices and drive the SYSRESET* signal if the board **is** the system controller. The RESET switch (S3) will reset all onboard devices except the DCAM and ECDM if the board **is not** the system controller. The VMEchip2 generates the SYSRESET* signal. The BusSwitch combines the VMEchip2 local reset, the power up reset, and the reset switch to generate a local board reset. Refer to the *Reset Module* section in the *BusSwitch* chapter for more information.

The ABORT switch (S2) can generate an interrupt to CPU0 via the NMI* signal. It is normally used to abort program execution and return to the debugger. This capability is controlled via the ABORT register in the BusSwitch.

The six LEDs on the MVME197 front panel are: FAIL, SCON, RUN, LAN, VME, and SCSI.

The yellow FAIL LED (DS1) is lit when the BRDFAIL signal line is active.

The green SCON LED (DS2) is lit when the VMEchip2 is the VMEbus system controller.

The green RUN LED (DS3) is lit when the MC88110 bus MC* pin is low.

The green LAN LED (DS4) lights when the LAN chip is the local peripheral bus master.

The green VME LED (DS5) lights when the board is using the VMEbus or when the board is accessed by the VMEbus.

The green SCSI LED (DS6) lights when the SCSI chip is the local peripheral bus master.

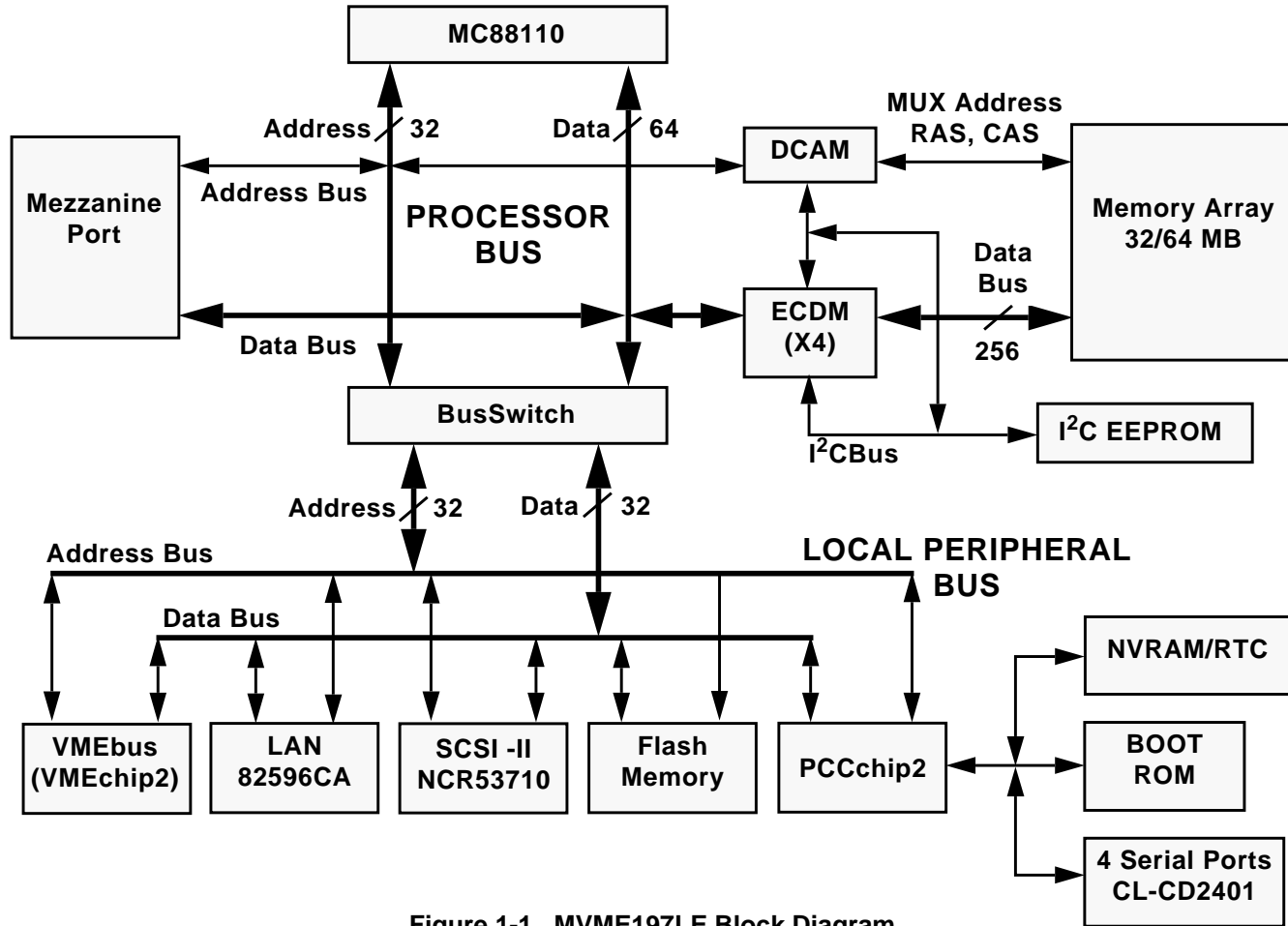


Figure 1-1. MVME197LE Block Diagram