128 channel high resolution TDC with integrated DAQ-system*

M. Traxler[1], D. Gil[2], M. Kajetanowicz[3], K. Korcyl[2], M. Palka[2], P. Salabura[2], P. Skott[1], R. Trebacz[2]
[1]EE, GSI, Darmstadt, Germany, [2]Jagiellonian University, Krakow, Poland, [3]Nowoczesna Elektronika, Krakow, Poland

A multi-purpose 128-channel Time to Digital Converter (TDC) electronics based on the HPTDC [1] with on-board DAQ functionality has been developed. The main usage will be the RPC-detector upgrade of the HADES-detector (2600 channels) with a needed time resolution of $< 100ps$ and the required possibility to measure the time of the rising and falling edge of the signal to make a Time-over-Threshold (TOT) measurement for a walk-correction of the RPC-detector. Additionally, it will be used for the Forward-Wall and Pion-Hodoscope upgrades (640 channels). The readout-electronics is on board and the data is transported via 100 MBit Ethernet and Internet-Protocol.

The Time to Digital Conversion of the 128 channels is done in 4 HPTDC chips (as shown in Fig. 1). The

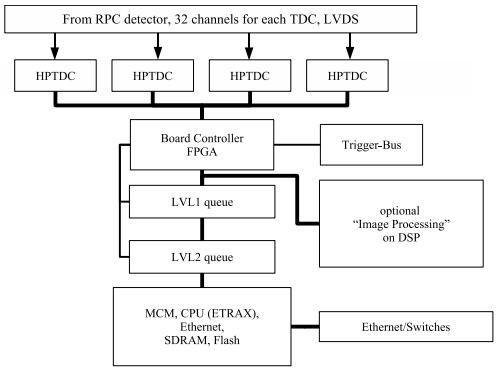

Figure 1: TDC Readout Board block diagram.

TDC-Readout-Board (TRB) has 4 input connectors (80-pins, high density), where each has 31 LVDS timing input signals and several I/O-signals for general purpose. The 32nd channel of each HPTC is connected to an external reference timing signal (LVDS). The HPTDC ASICs are highly configurable [1] and allow to choose the TDC bin-width in the range of $780ps$ and $25ps$ (at $25ps$ one only has $1/4$ of the channels available), detect rising and falling edge of the timing-signal and allow to define a matching-window, so that delay cables are not necessary anymore. An external trigger signal starts the selection of data in the HPTDCs and the board-controller FPGA initiates the readout. This data is then first stored in a FIFO (128 kB) where it is waiting for an external LVL2 trigger decision, which decides if the data can be discarded or has to be transported to mass storage (the LVL2 trigger is needed for the HADES DAQ but optional). If the trigger was positive, the data is stored in a second memory (128 kB) and then readout by a single chip computer (ETRAX [2]) with linux running on it. Then the data is formatted and transported via UDP over 100MBit Ethernet to the event-builder, which collects and orders the data from many different sources. The UDP transport performance of the ETRAX has been measured to be 4 MB/s [3]. Having the DAQ-system with a full featured computer so close to the FEE allows the implementation of the slow-control on the TRB (EPICS), e.g. for setting the thresholds of the attached FEE. The TRB uses a 48V galvanic isolated power-supply which simplifies power-distribution, prevents ground-loops and allows to mount the TRB directly on the detector. The time resolution between two reference channels (different HPTDCs) resulted ($100ps$ bining) in $\sigma = 40ps$, as expected from the known HPTDC performance. Great care has been taken for the layout of the PCB to assure impedance matched and decoupled transmission lines of the LVDS-timing signals, which is rewarded in a crosstalk influence to the resolution of less than $20ps$ (preliminary result, still under test).

In November 2005 a full system RPC-beam-test was performed, which included the full electronics chain with detector, FEE, TRB and beam in the HADES-cave. An integral time resolution of $\sigma = 80ps$ has been reached, without any corrections (Fig. 2, for details see [4]). The TRB

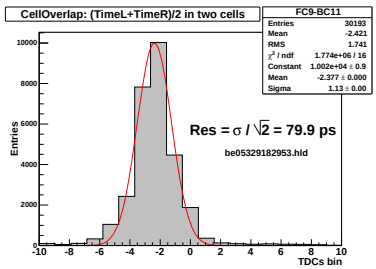

Figure 2: Time resolution of full electronics chain.

(without any speed optimizations) was fully integrated into the HADES-DAQ system and running stably with up to 31 kHz LVL1 and 2 kHz LVL2 rate, which corresponds to 1.2 MB/s with the given occupancy.

References

[1] HPTDC, J. Christiansen, Digital Microelec. Group, CERN
[2] ETRAX, AXIS Communications, Sweden
[3] R. Trebacz, Single-Chip-Linux-Computer for the HADES-experiment Data-Acquisition, GSI Summer Student Programm 2004
[4] J.S. Lange, Status of the HADES RPC Project, GSI Scientific Report, 2006

*Work supported by EU FP6 grant, contract number 515876 and EU FP6 grant RII3-CT-2004-5060781 (JRA1)