S390: In-beam test of the prototype AIDA detector system for DESPEC

presented by

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on behalf of the AIDA collaboration

(Edinburgh – Liverpool – STFC DL & RAL)

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AIDA Project

Project web site

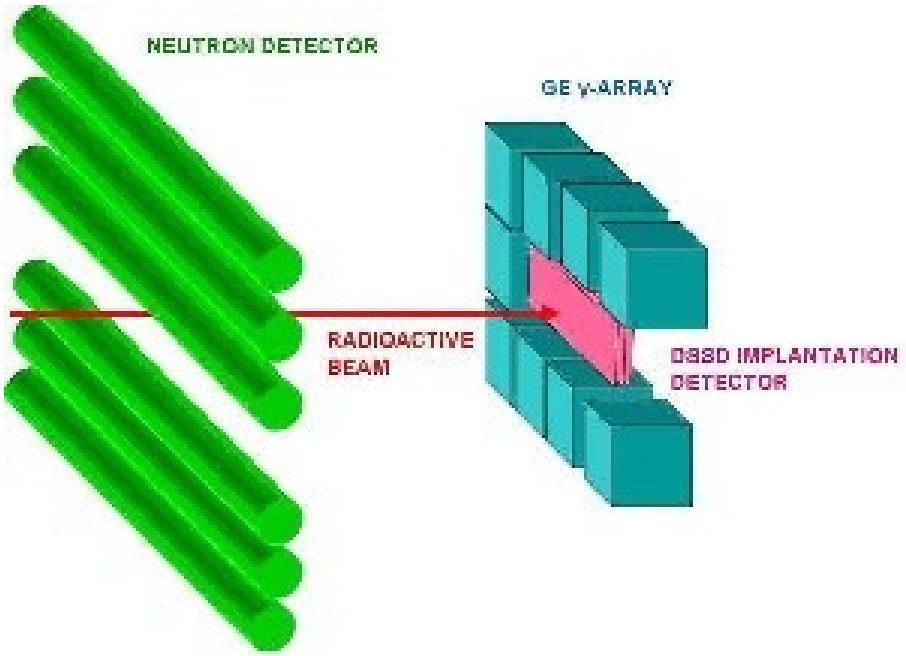
http://www.ph.ed.ac.uk/~td/AIDA/welcome.html

The University of Edinburgh (lead RO)
Phil Woods *et al.*
The University of Liverpool
Rob Page *et al.*
STFC DL & RAL
John Simpson *et al.*

Project Manager: Tom Davinson

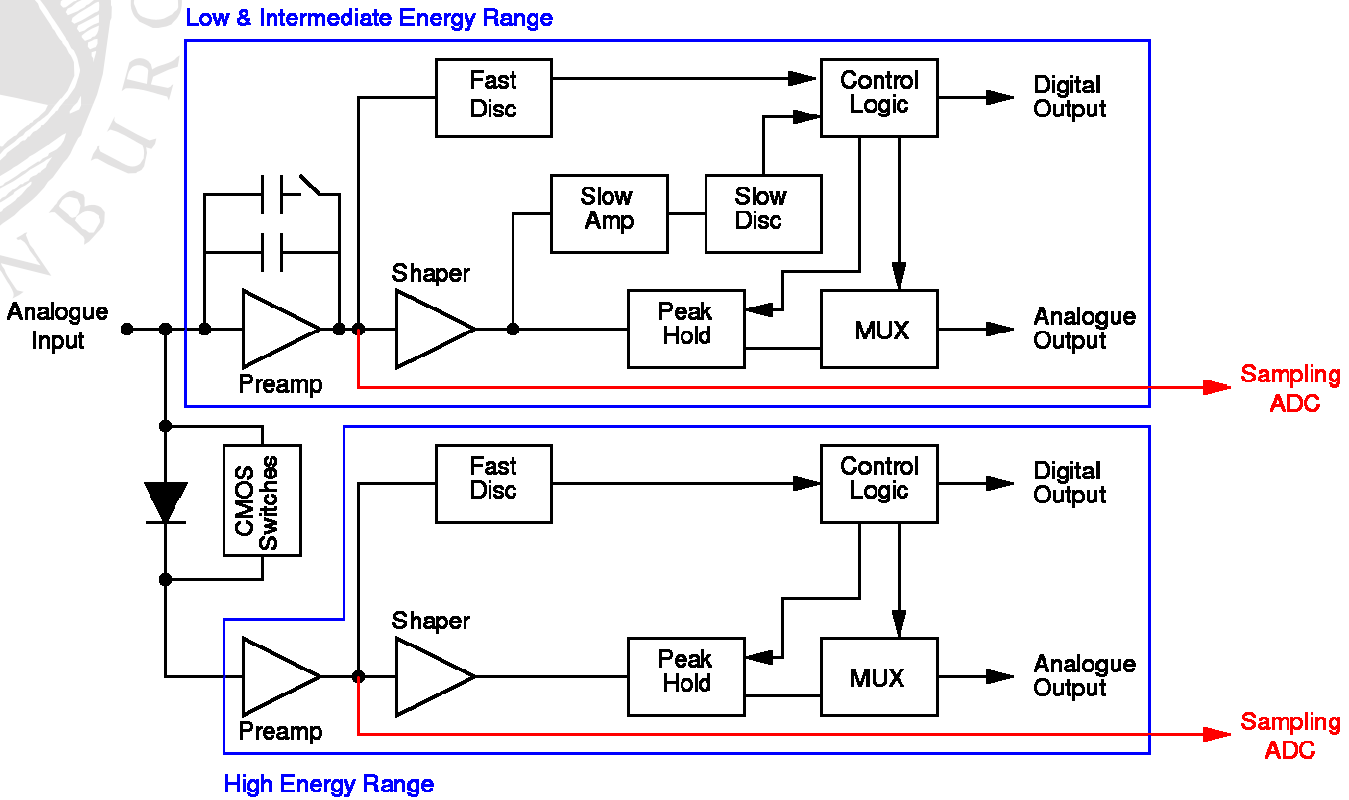
Project commenced: September 2006

DESPEC: Implantation DSSD Concept



- SuperFRS, Low Energy Branch (LEB)
- Exotic nuclei – energies ~ 50 – 200MeV/u
- Implanted into multi-plane, highly segmented DSSD array
- Implant – decay correlations
- Multi-GeV DSSD implantation events
- Observe subsequent p, 2p, α, β, γ, βp, βn … decays
- Measure half lives, branching ratios, decay energies …
- Tag interesting events for gamma and neutron detector arrays

Schematic of Prototype ASIC Functionality



Note – *prototype* ASIC will also evaluate use of digital signal processing

Potential advantages

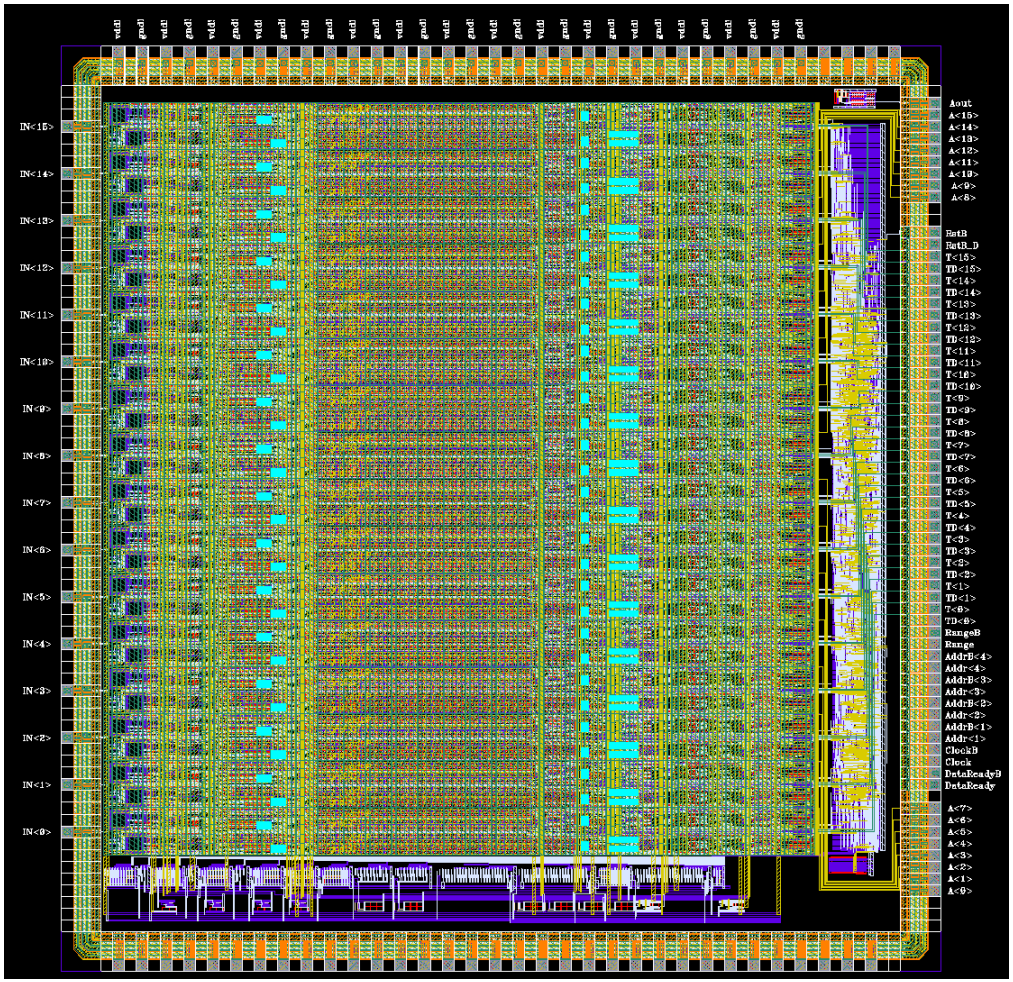
- decay – decay correlations to ~ 200ns
- pulse shape analysis
- ballistic deficit correction

Prototype AIDA ASIC: Top level design

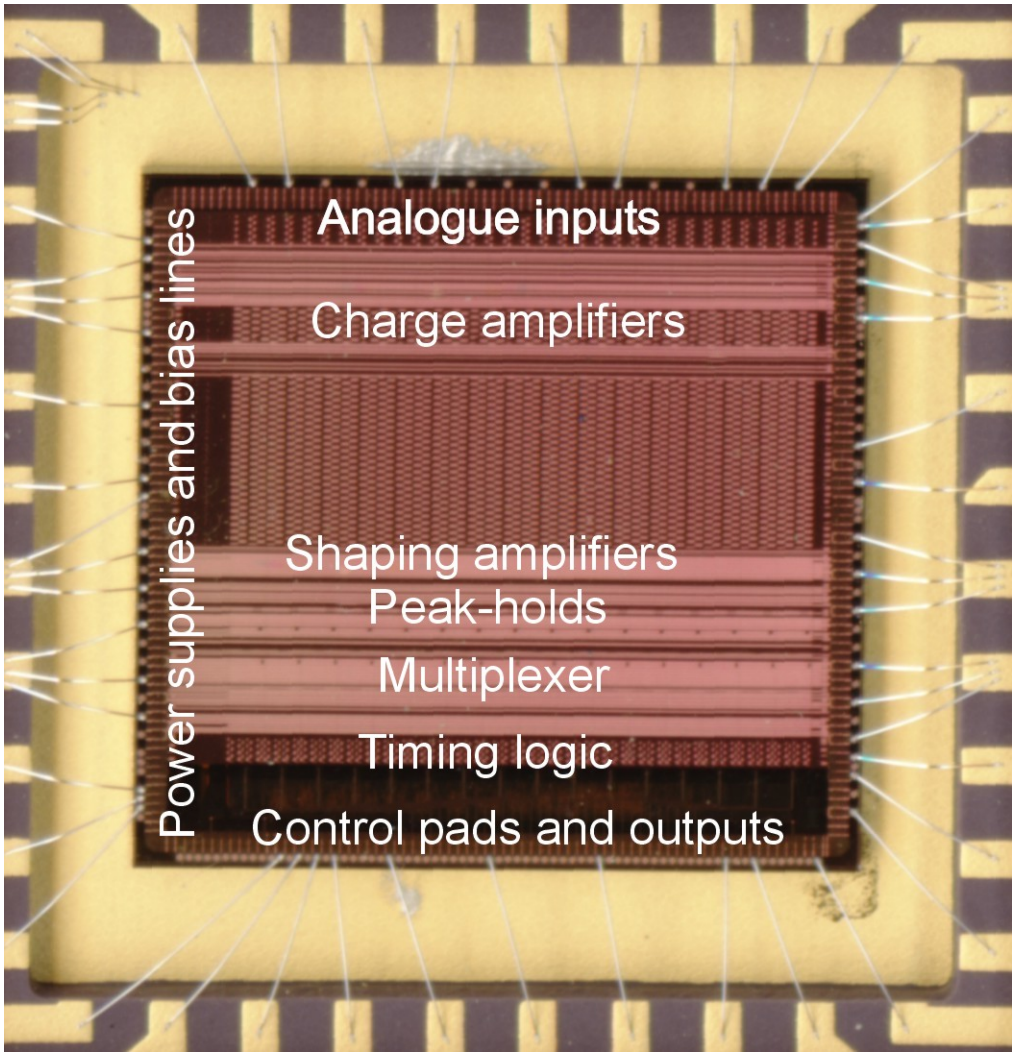
- Analogue inputs left edge
- Control/outputs right edge
- Power/bias top and bottom
- 16 channels per ASIC

- Prototypes delivered May 2009
  - MPW run
  - 100 dies delivered

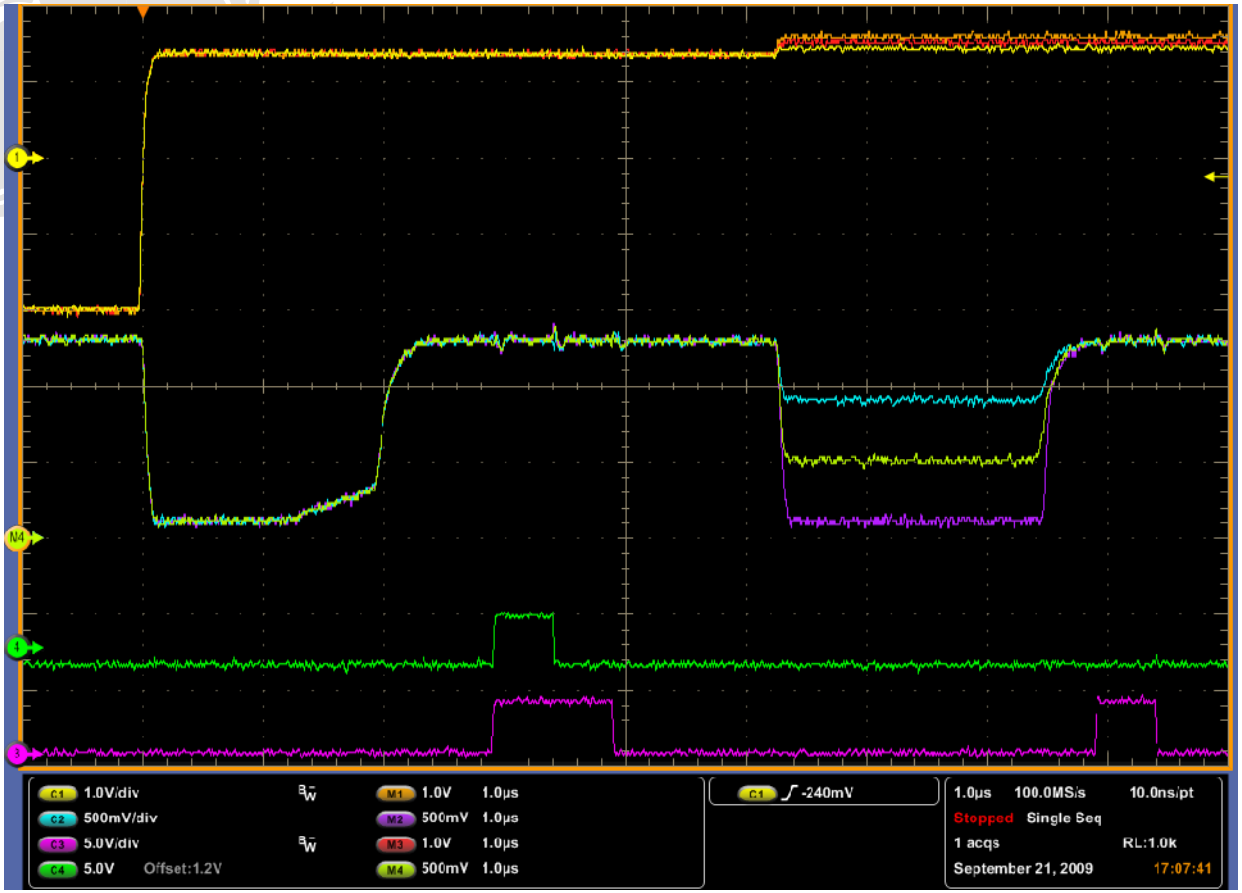
- Functional tests at STFC RAL OK



Prototype AIDA ASIC



3: High Energy (HE) + ME



Input signals (voltage step capacitive-coupled)

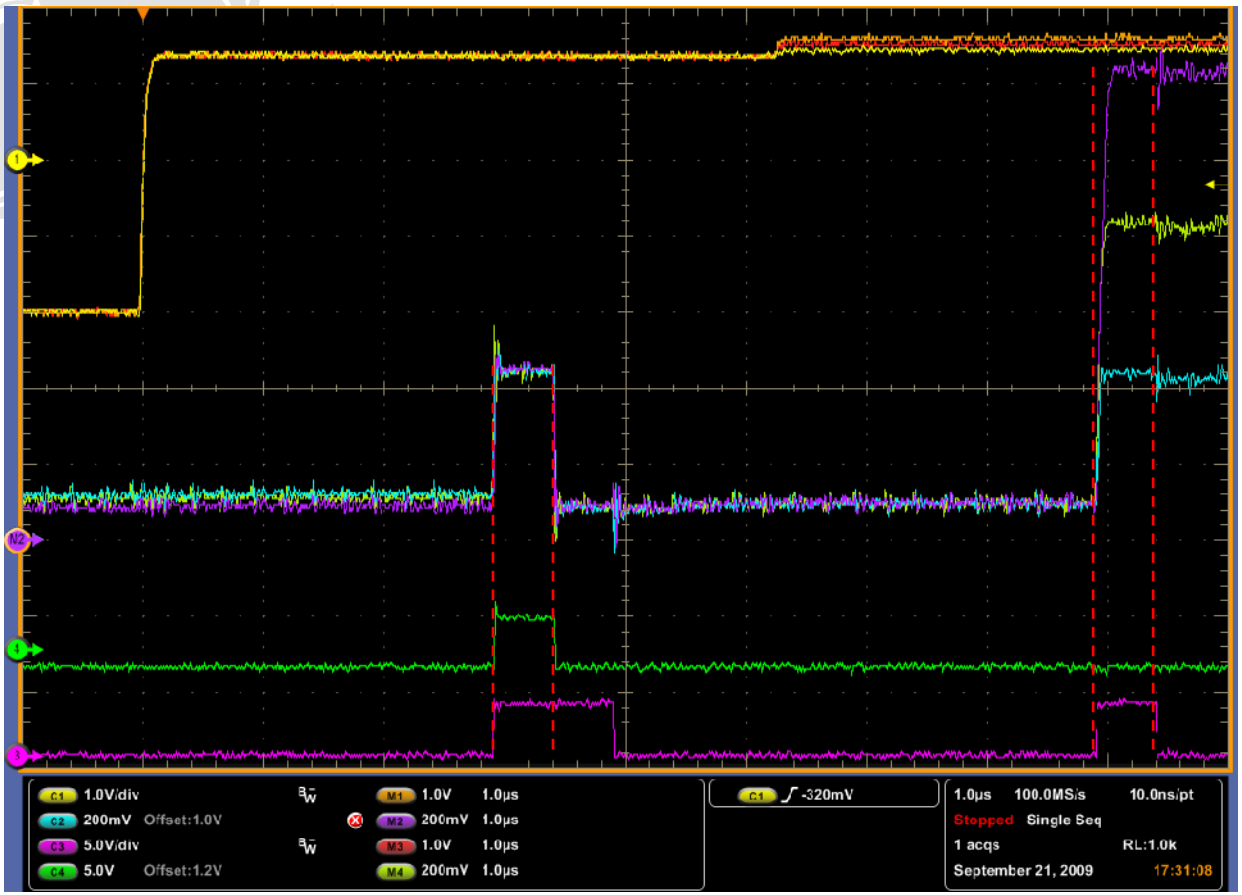
Preamp buffered output (Low-Medium Energy Channel)

“Range” signal
High = high-energy channel active

“Data Ready” signal

Fixed high-energy (HE) event (610pC) followed by three ME events (15pC, 30pC, 45pC): the ASIC recovers autonomously from the overload of the L-ME channel and the second event is read correctly.

3: High Energy (HE) + ME



Input signals (voltage step capacitive-coupled)

Analog output (peak-hold multiplexed output)

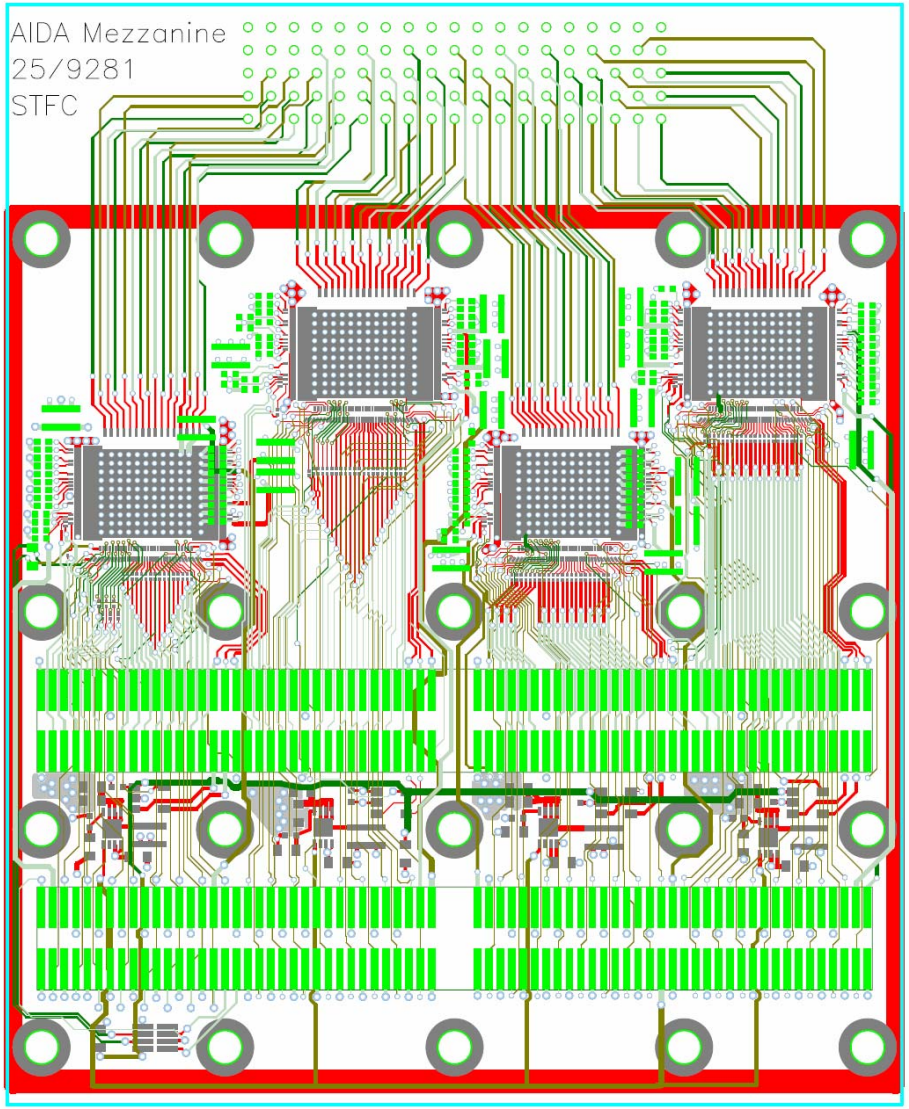
“Range” signal
High = high-energy channel active

“Data Ready” signal

First value (constant) given by the High-Energy channel, second by the Medium-Energy channel.

Prototype AIDA Mezzanine

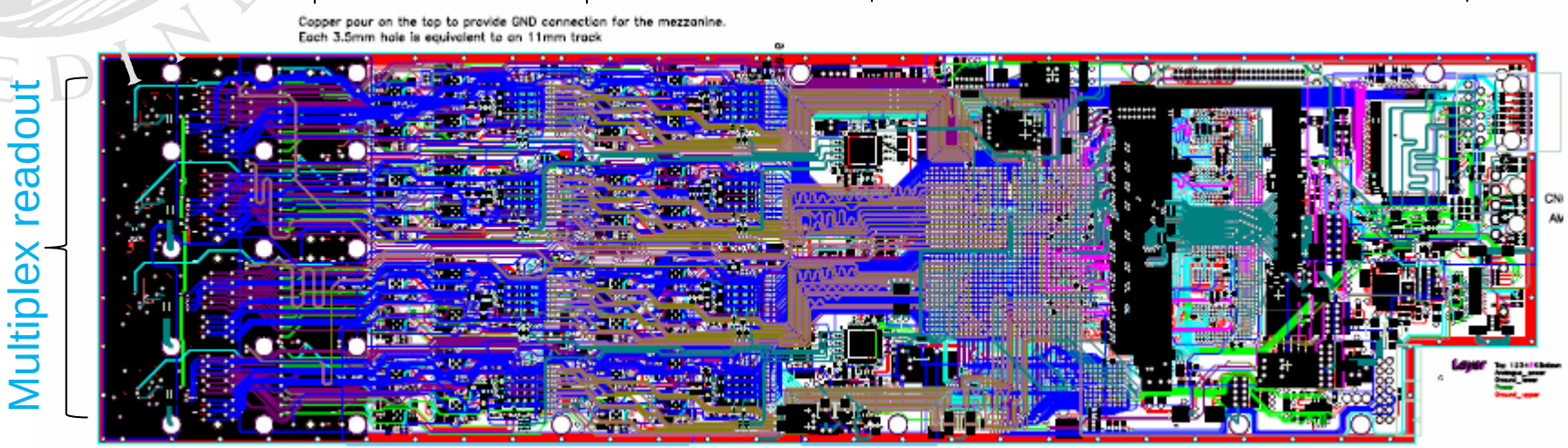
- 4x AIDA ASICs
  64 channels
- Design complete
- Delivery November 9
  20 units



Prototype AIDA FEE

Digital readout

FPGA, Memory, Gbit



Mezzanine

Clock distribution

Power Supplies

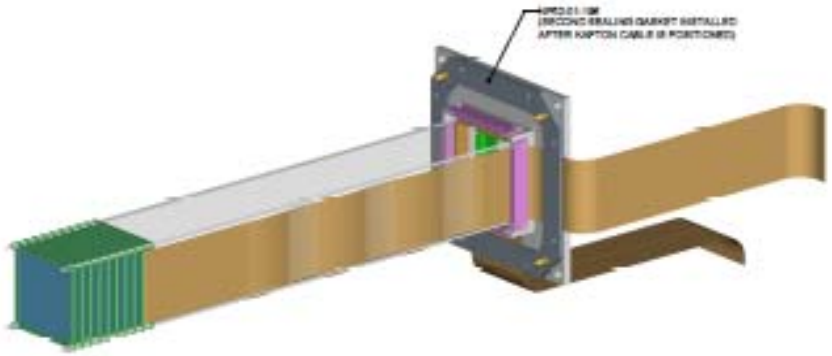
- Design complete
- Production complete

  8 units (4x AIDA, 2x DL DDG, 2x LYCCA)
- Delivered week commencing 21.9.09

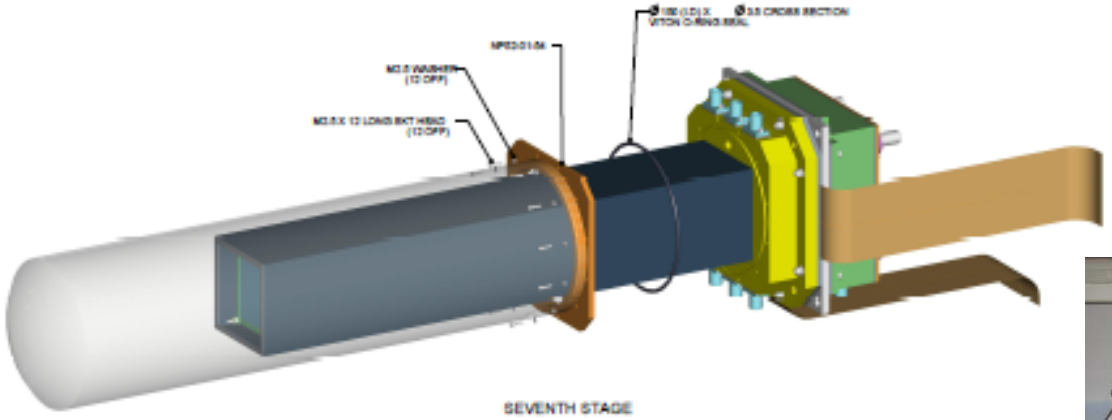
Prototype FEE card

- Initial tests underway (STFC DL DDG)
  - FPGA Virtex 5 configuration
  - PowerPC with internal memory & terminal
  - DDR2 memory tests
  - Gbit ethernet
  - ASIC comms and discriminator timing
  - Analog buffers & ADCs
  - etc

Prototype AIDA Enclosure



SECOND STAGE



SEVENTH STAGE

- Design drawings (PDF) available
  http://www.eng.dl.ac.uk/secure/np-work/AIDA/

AIDA Project Timeline

- November/December 2009
  Systems integration (ASIC+Mezzanine+FEE)
  Bench tests

- February 2010
  Prototype AIDA hardware available for in-beam tests

- 2010
  Design revisions & production

- February 2011
  End of grant period

S390

System bench tests (radioactive sources & pulser)

energy & time resolution, linearity, min.discriminator threshold etc

System in-beam tests

high energy implants – multiplicity, crosstalk, energy resolution etc.

ASIC parameters – optimise programmable reset sequence
(minimise overload recovery time)

characterise overload recovery – design revision

S390

- ^{238}U or ^{124}Xe primary beam
- FRS selects species with fast (~μs) decays
  $^{219\text{-}223}$U, $^{218\text{-}221}$Pa, $^{216\text{-}220}$Th or ^{109}I or ^{106}Te
- beam request

1 shift	FRS setup
2 shifts	FRS detector calibration etc
2 shifts	AIDA system response to high energy implants
9 shifts	evaluate & optimise overload recovery using fast implant-decay correlations
1 shift	fast decay-decay correlations

Acknowledgements

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