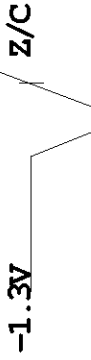


LOGIC LEVEL DIAGRAM



ECL VOUT1-A DT: 2US

ECL VOUT1-AB

ECL VOUT2-A W: 50ns

ECL VOUT2-AB

ECL VOUT1-B DT: 2US

ECL VOUT1-BB

ECL VOUT2-B W: 50ns

ECL VOUT2-BB

ECL VOUT1-C DT: 2US

ECL VOUT1-CB

ECL VOUT2-C W: 50ns

ECL VOUT2-CB

ECL VOUT1-D DT: 2US

ECL VOUT1-DB

ECL VOUT2-D W: 50ns

ECL VOUT2-DB

ECL ACS-AB ^{B\} 500NS

ECL U11C Q 2AB.2BB.2CB.2DB=Q

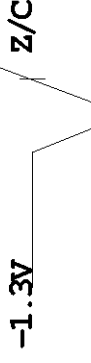
ECL W=50ns U11-D,Q TR=100ns ^A _{TR=100ns}

ECL Q = A.B\

ECL/F-NIM Td=200-800ns W=50n IDC

ECL/F-NIM 500ns MPC

LOGIC LEVEL DIAGRAM



TTL VOUT1-A DT: 2US

TTL VOUT2-A W: 50ns

TTL VOUT1-B DT: 2US

TTL VOUT2-B W: 50ns

TTL VOUT1-C DT: 2US

TTL VOUT2-C W: 50ns

TTL VOUT1-D DT: 2US

TTL VOUT2-D W: 50ns

TTL DT: 10us

TTL DT: 10us