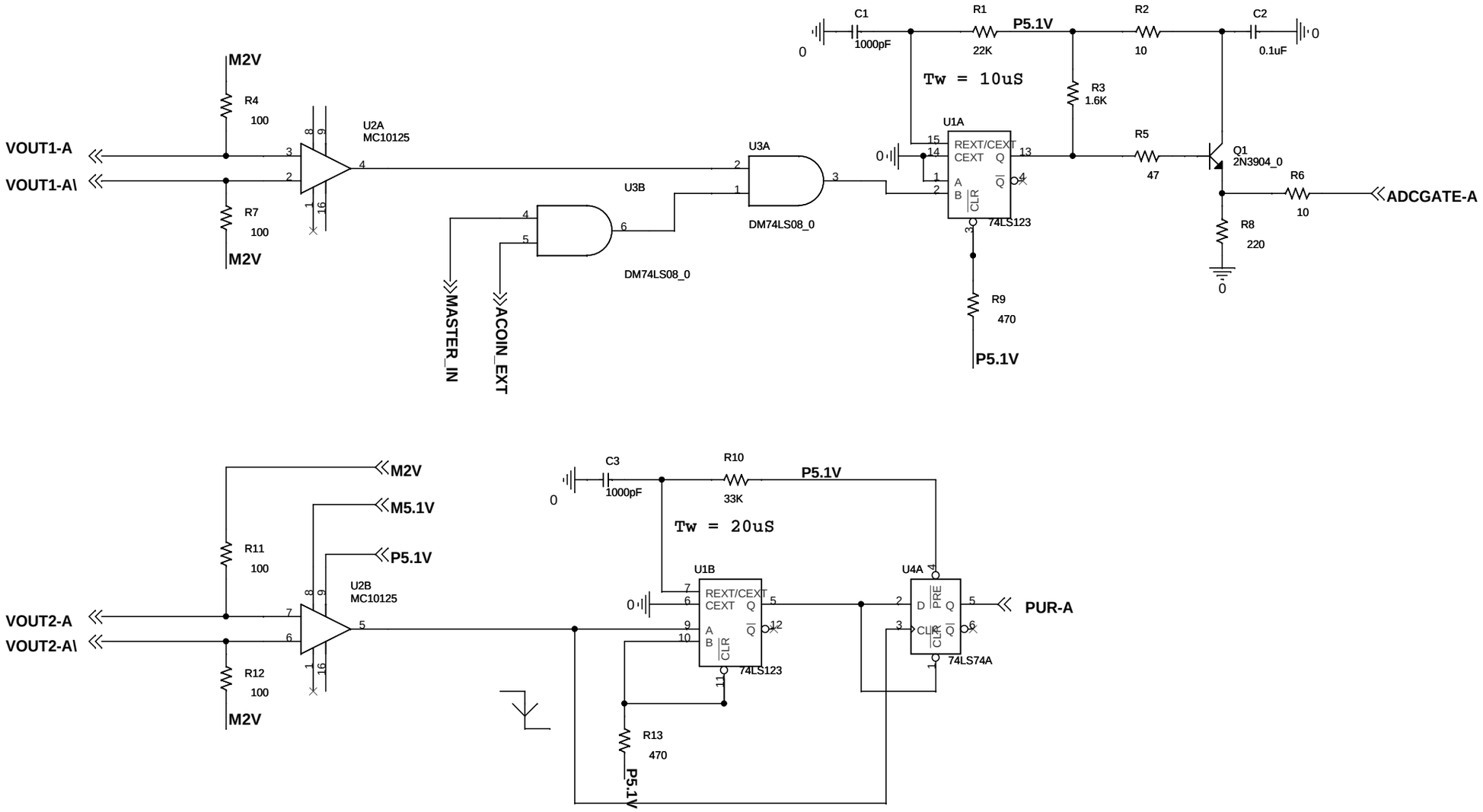

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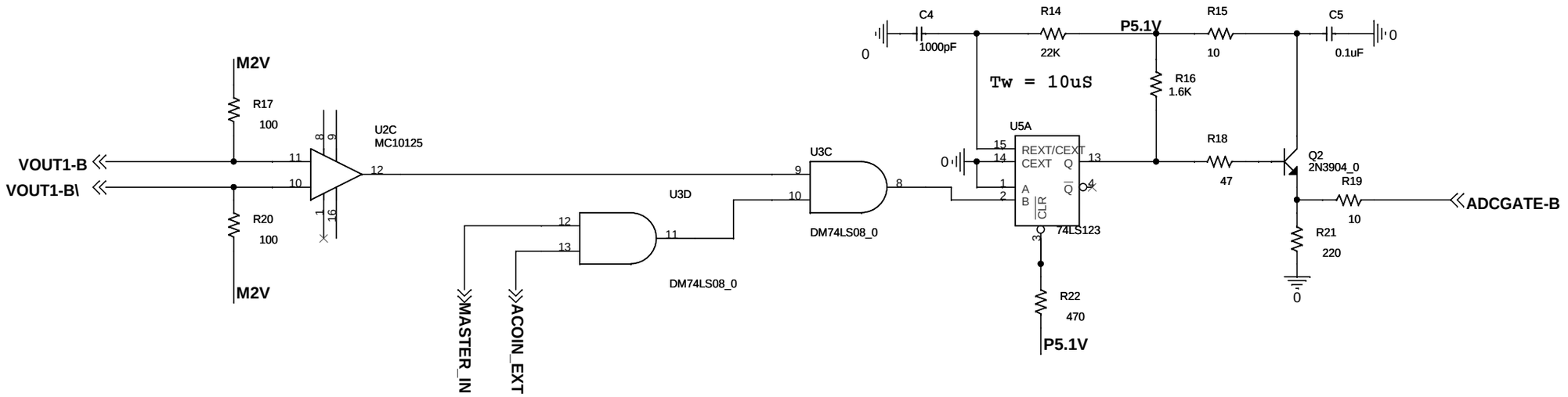

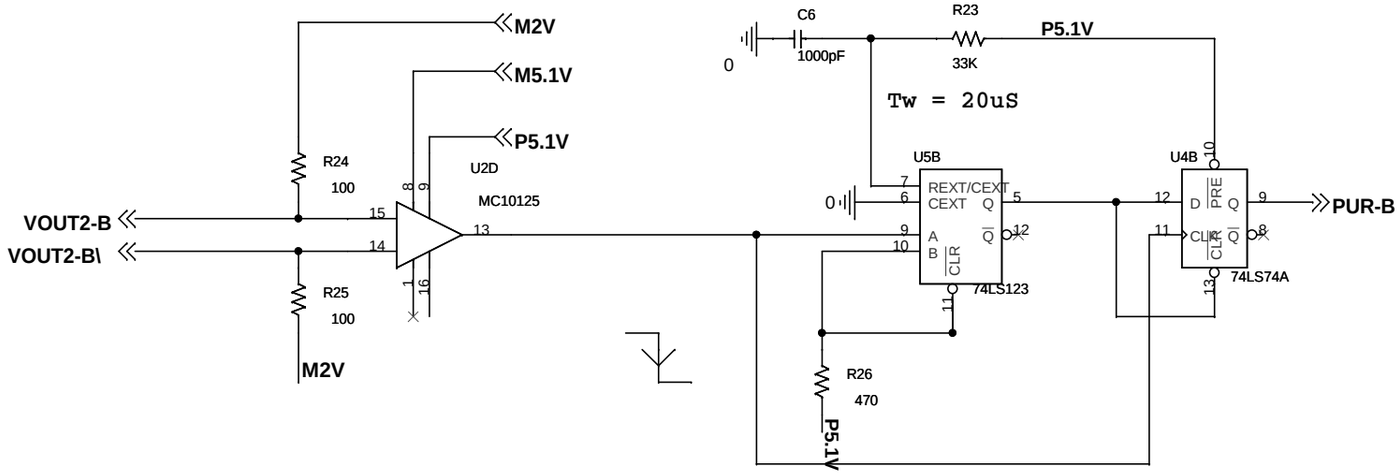

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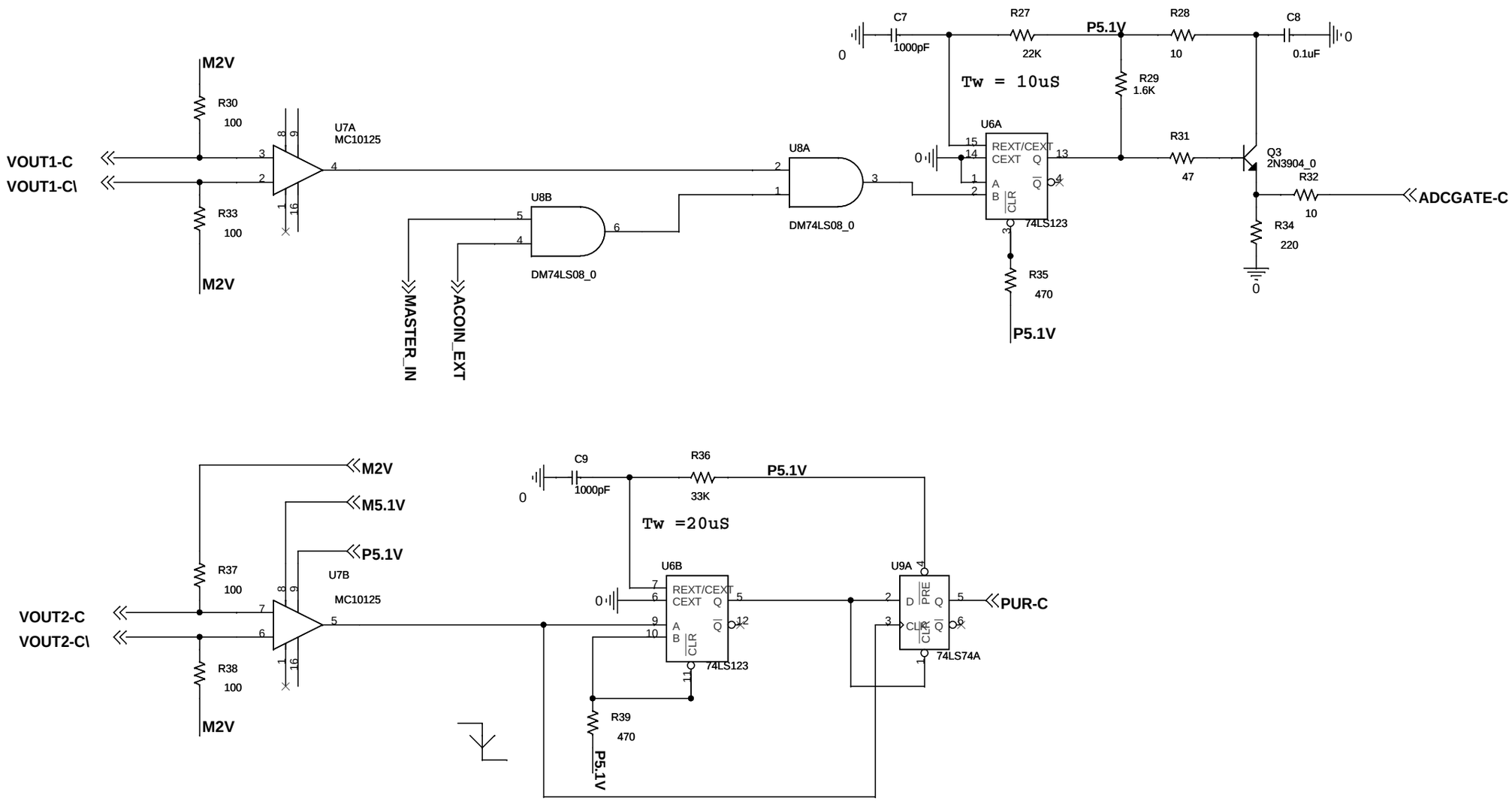

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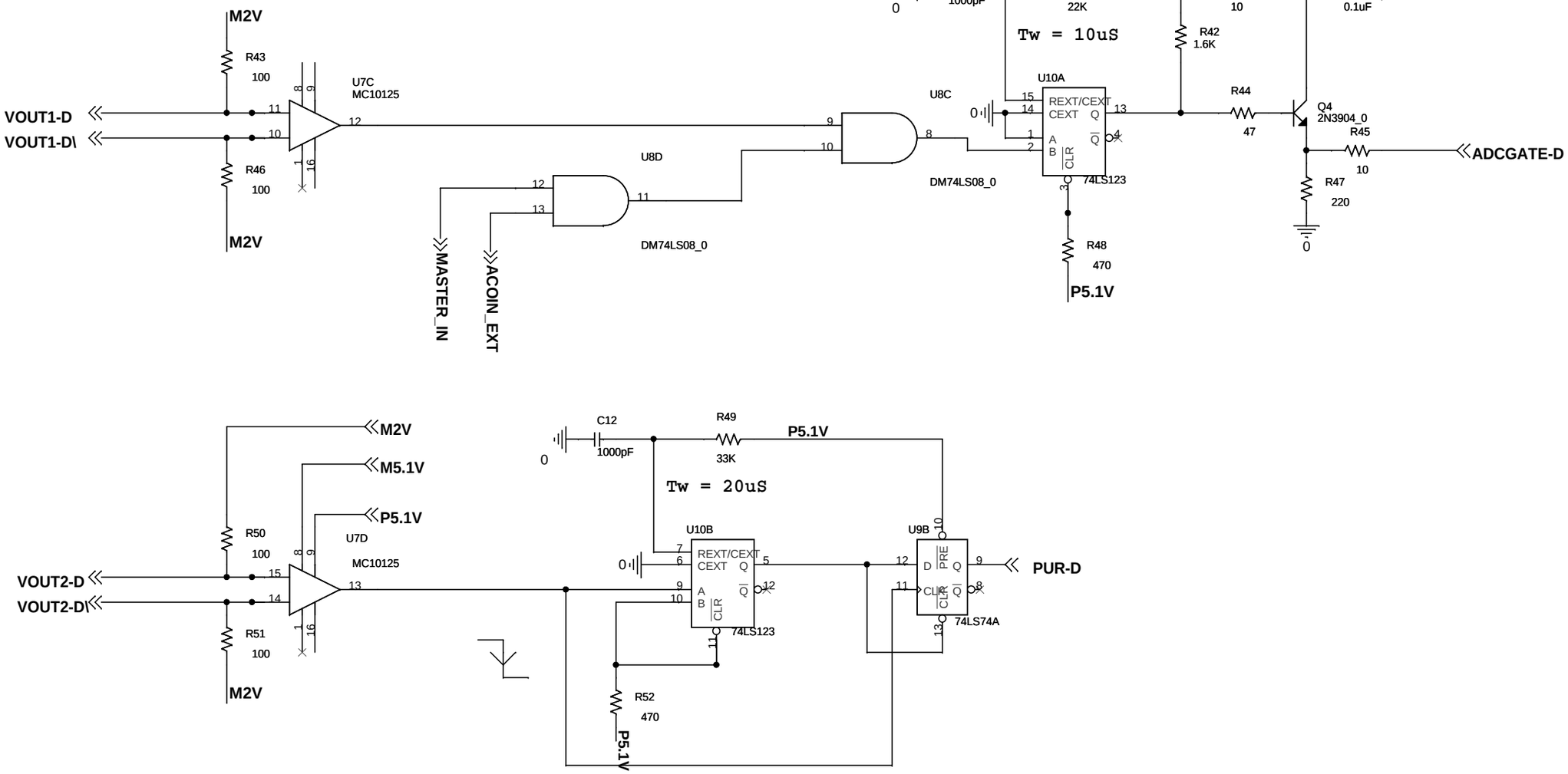

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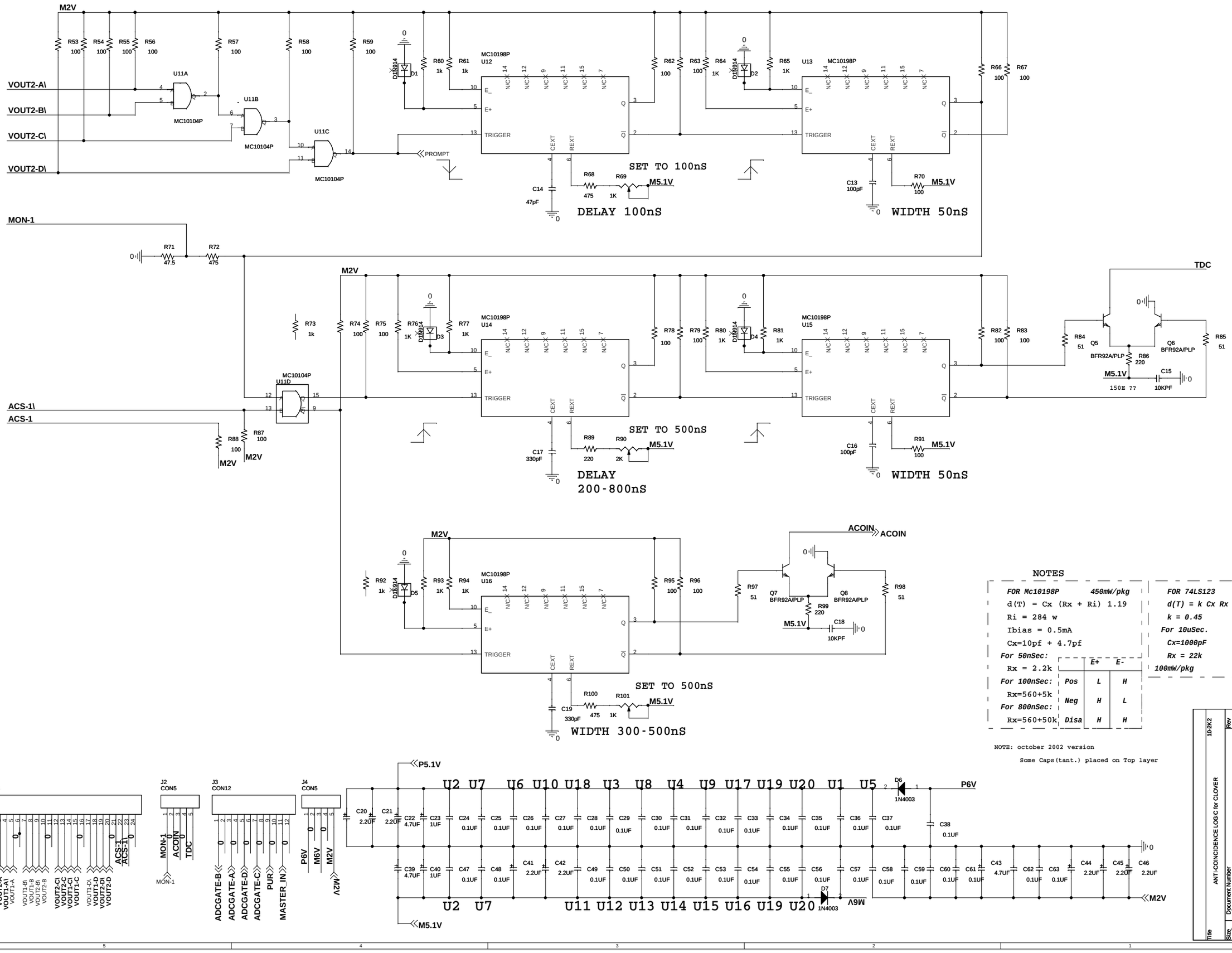

NOTES

FOR Mc10198P 450mW/pkg		FOR 74LS123
d(T) = Cx (Rx + Ri) 1.19		d(T) = k Cx Rx
Ri = 284 w		k = 0.45
Ibias = 0.5mA		For 10uSec.
Cx=10pf + 4.7pf		Cx=1000pF
For 50nSec:		Rx = 22k
Rx = 2.2k		100mW/pkg

	E+	E-
For 100nSec:	Pos	L	H
Rx=560+5k	Neg	H	L
For 800nSec:	Disa	H	H
Rx=560+50k			

NOTE: october 2002 version

Some Caps(tant.) placed on Top layer

Title	10-2K2 ANTI-COINCIDENCE LOGIC for CLOVER
Size	C
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Rev	
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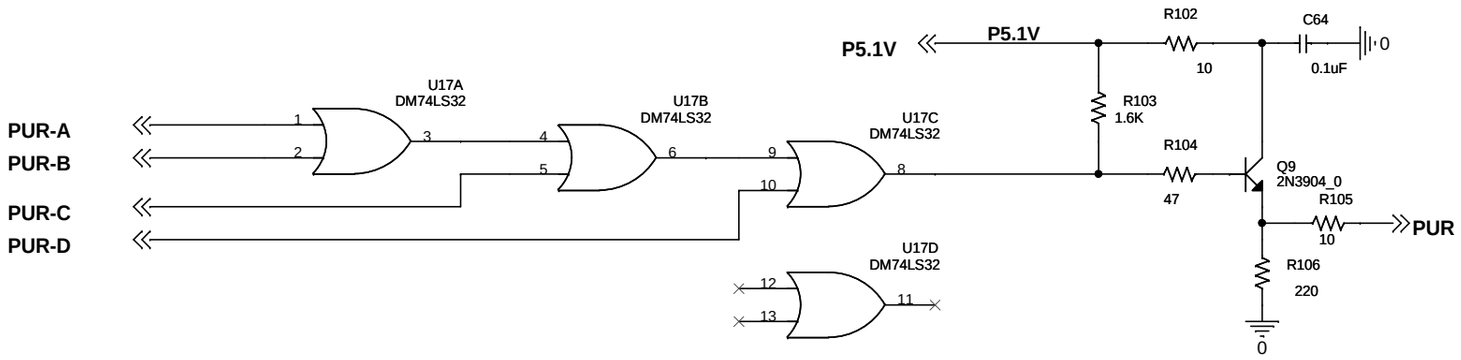

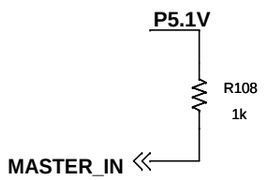

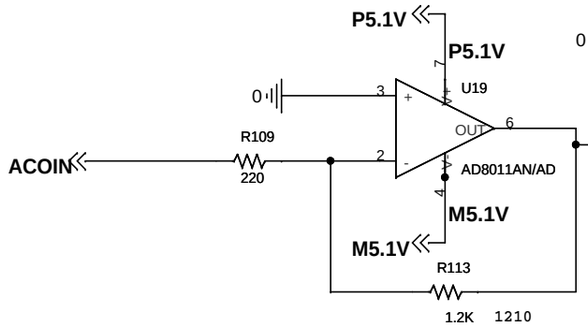

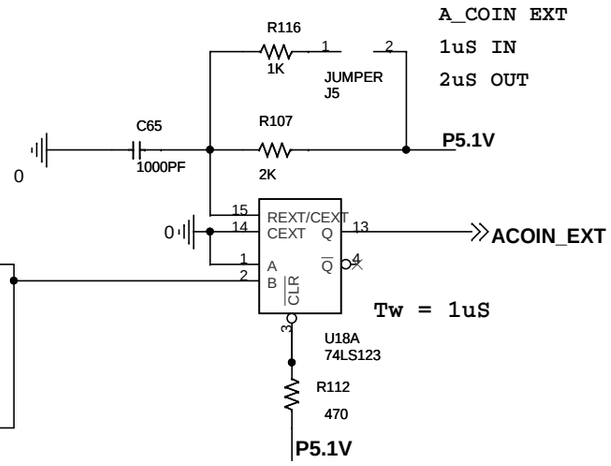

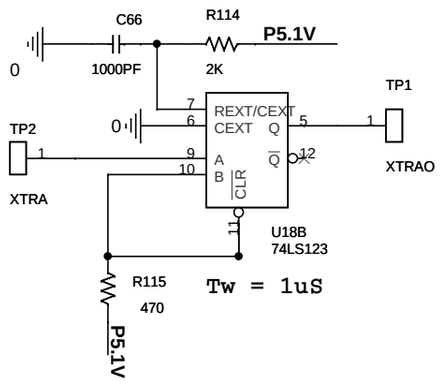

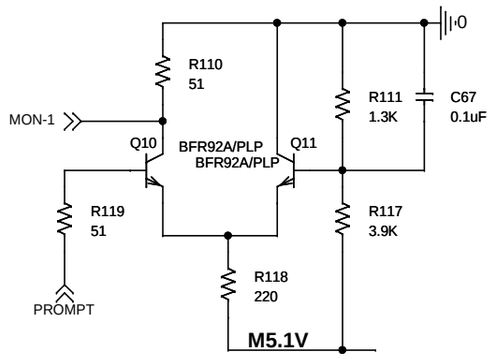

Title: ANTI-COINCIDENCE LOGIC for CLOVER		
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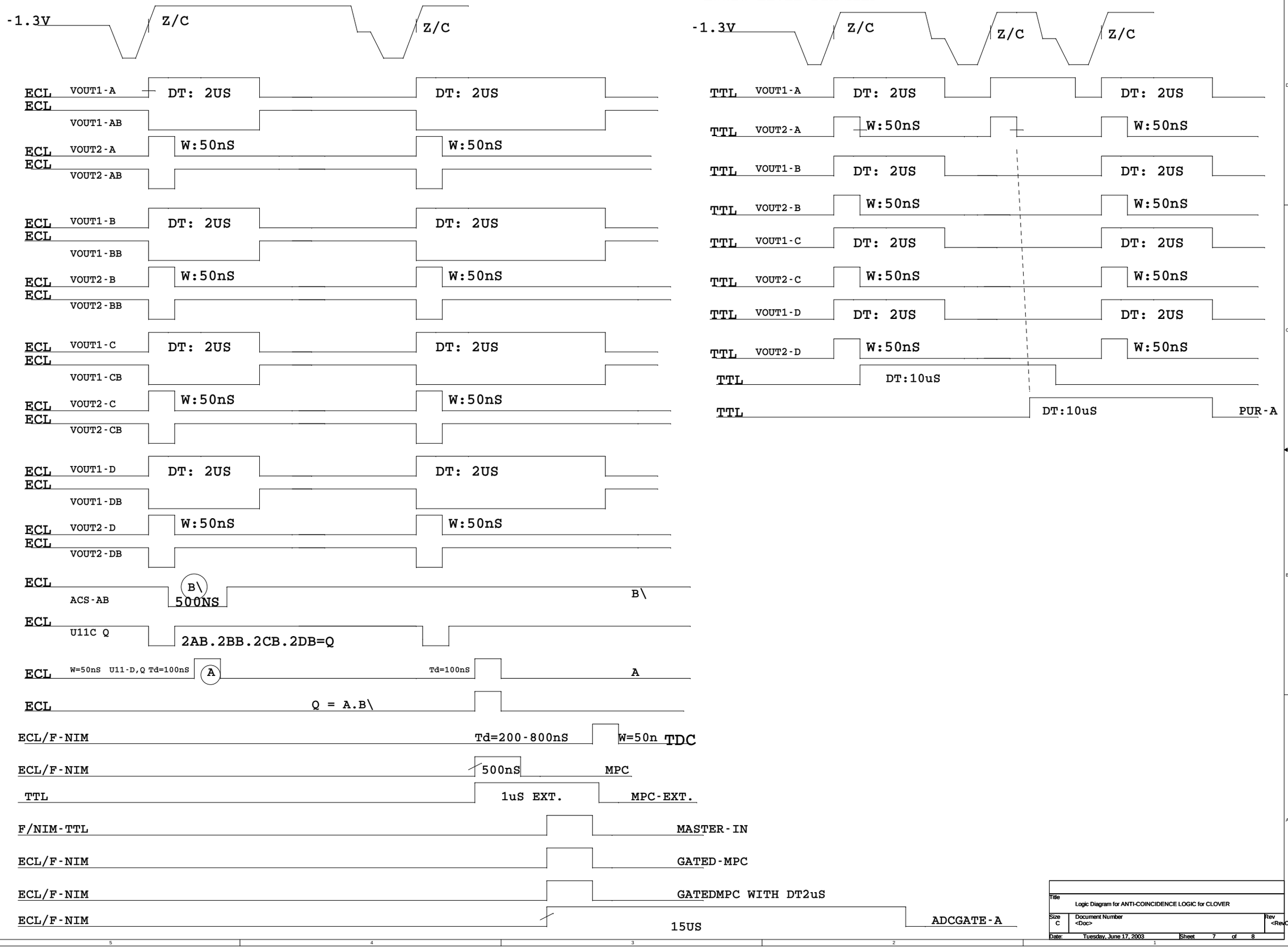
LOGIC LEVEL DIAGRAM



LOGIC LEVEL DIAGRAM

Title	Logic Diagram for ANTI-COINCIDENCE LOGIC for CLOVER	
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WATH adj.

TFA
G=~15
Td=200nS
Ti=NONE
SRT/CFD
DT=2uS
CFD
W=50nS
P/Z_COMP
DC ADJ.
WALK_ADJ.
VOUT1_A
VOUT2_A
ECL TO TTL
AND
10uS MONOSHOT
TTL
ADC GATE A
PILE_UP REJECTION
20uS
PUR_A
PUR_A
PUR_B
PUR_C
PUR_D
OR
PUR
TFA
G=~15
Td=200nS
Ti=NONE
SRT/CFD
DT=2uS
CFD
W=50nS
P/Z_COMP
LLTH
DC ADJ.
WALK_ADJ.
VOUT1_B
VOUT2_B
ECL TO TTL
AND
10uS MONOSHOT
TTL
ADC GATE B
PILE_UP REJECTION
20uS
PUR_B
OR
DELAY
100nS
WIDTH
50nS
TFA
G=~15
Td=200nS
TI=NONE
SRT/CFD
DT=2uS
CFD
W=50nS
P/Z_COMP
LLTH
DC ADJ.
WALK_ADJ.
VOUT1_C
VOUT2_C
ECL TO TTL
AND
10uS MONOSHOT
TTL
ADC GATE C
PILE_UP REJECTION
20uS
PUR_C
ACOIN_EXT
1uS MONOSHOT
F/NIM TO TTL
TFA
G=~15
Td=200nS
TI=NONE
SRT/CFD
DT=2uS
CFD
W=50nS
P/Z_COMP
LLTH
DC ADJ.
WALK_ADJ.
VOUT1_D
VOUT2_D
ECL TO TTL
AND
10uS MONOSHOT
TTL
ADC GATE D
PILE_UP REJECTION
20uS
PUR_D
AND
WIDTH
300-500nS
ECL TO F/NIM
ACOIN
ACOIN_EXT
FROM MASTER GATE
TFA
G=~15
Td=200nS
TI=NONE
SRT/CFD
CFD
W=500nS
P/Z_COMP
LLTH
DC ADJ.
WALK adj.
ACS_1
ECL
DELAY
200-800nS
WIDTH
50nS
ECL TO F/NIM
TO TDC

File	Block digram of Compton Suppression Logic for CLOVER ARRAY	
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