TECHNICAL REPORT

TITLE	**:Technical Report on Clover Electronics Module**
AUTHORS	**: S.Venkataramanan*, Arti Gupta, Kusum Rani, R.P.Singh, S.Muralithar, B.P.Ajith Kumar, R.K.Bhowmik**
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NUCLEAR SCIENCE CENTRE

(An Autonomous Inter-University Centre of UGC)

Post Box No.: 10502, Aruna Asaf Ali Marg,

New Delhi 110067 (India) Phone: 2689 3955, 2689 2603, 2689 2601

Fax: 091-11-2689 3666 Email: info@nsc.res.in

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TECHNICAL REPORT

ON

CLOVER ELECTRONICS MODULE

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Prepared by

ELECTRONICS LABORATORY

NUCLEAR SCIENCE CENTRE
NEW DELHI 110067.

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CLOVER ELECTRONICS MODULE

S.Venkataramanan*, Arti Gupta, Kusum Rani, R.P.Singh,
S.Muralithar, B.P.Ajith Kumar, R.K.Bhowmik

*email: venkat@nsc.ernet.in

Abstract:

A proptotype NIM module containing Shaping amplifiers, TFAs, CFDs and logic circuitry for processing signals from a Clover detector with Anti Compton Shield (ACS) has been developed. The circuits are realised in High density daughter card form using SMD components, while keeping the features and specifications at par with commercially available modules. Two numbers of Pre-production modules are assembled and being successfully used inbeam with INGA-HIRA setup.

Version:

Current version includes some added features in ACLogic card and F_NIM outputs are available from all CFDs in rear panel. This manual supersedes all previous versions.

Acknowledgment

We would like to thank Engineer and Scientists from GIP, Ganil, France for their constant support in simulating various circuit blocks and for fruitful discussions. Our sincere thanks to Dr.Amit Roy, Prof. G.K.Mehta for their constant encouragement and providing the necessary infrastructure inorder to complete this project successfully. We also thank M/s.ANCOMP for their help in providing good quality PCBs. Our sincere thanks to TIFAC (DST) for initiating patent filing procedure in short time.

Introduction

The experimental facility like INGA consists of a large number of HPGe detectors. Each channel requires a Spectroscopy amplifier, Timing Filter Amplifier (TFA) and Constant Fraction Discriminator (CFD) and associated Logic circuits. Typical commercial electronic setup would require a large number of modules which occupy large area, interconnecting cables and connectors. The NIM module developed at NSC contains five channels of electronics to accommodate one clover with accompanying anti-Compton shield. The content of this double width NIM module is shown in fig 1.

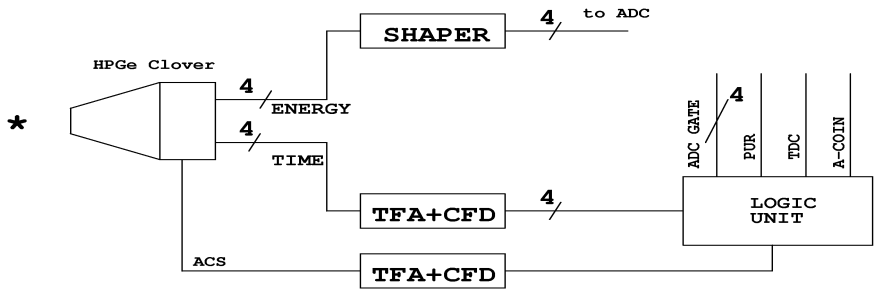


Fig:1 Clover Electronics Bolock Diagram

The high resolution spectroscopy amplifiers have fixed 3μs shaping constant and 3 fixed gain settings (2, 4 & 6 MeV) which are jumper selectable. The DC baseline is stabilized with Gated BLR, while P/Z and BLR (manual) threshold adjustments can be remotely voltage controlled. The unipolar output has the dynamic range of 8 volts across 50 ohms.

Four TFAs with fixed time constants and gain settings are provided for processing TIMING signals from Clover detector. The TFA is designed with single CFA gain stage and baseline is stabilized with twin diode restorer and high input impedence buffer. These amplifiers have rise time of better than 10 ns across their dynamic range of ±2.5 volts across 100 ohms. The CF Discriminator with amplitude & risetime compensation (ARC) is realized with fixed delay of 25 ns and fraction of 0.3. The Lower Level Threshold, WALK adjustment and Monitoring are possible on front panel. The CFD outputs from the individual Clover elements with width of 50 ns and dead time of 2 μs are set internally.

Anti-compton shield signal received from ACS Preamplifier is processed with identical TFA + CFD as mentioned above but without dead time. The raw timing logic signals received from CFDs from Clover detector and ACS detector are further processed to affect Anti-coincidence. The TFA and CFD outputs from the ACS are available on the panel for ease of adjustment. The logic functions performed are Pileup Rejection, Individual ADC GATing, Anti-Coincidence output and Delayed STOP signal for TDC. All these logic outputs are buffered and available in standard logic levels on the panel.

Principle of Operations

The INGA Clover Electronics Module is essentially a double width NIM module contains a mother board where individual blocks in daughter card form are inserted. The DC supply lines are filtered with PI filter section, and a negative 2V zener regulated supply is generated. The rear panel receives the inputs like "ENERGY" and "TIME" signals from Preamplifier through Lemo (00 series) connectors. The Front panel provides the various monitoring points like P/Z Mon., BUSY, WALK_MON, Energy OUT, ADC GATE and other Logic related signals (TDC STOP, ACOIN..) through Lemo connectors and manual control of various adjustment like P/Z Adj., BLR Threshold adj., WALK adj., LLTH adj., through multiturn potentiometers. The TFA (ACS) and CFD (F_NIM) outputs corresponding to clover elements are provided for monitoring. The panel layout can be seen in attached photograph or drawing.

The high frequency signal layout techniques are widely used for reduction of ground loop related and pick-up problems in the motherboard. RG178C/U coaxial cable is used for interconnection along with ground cap with Lemo-00 series connectors. Typical cable lengths used for various interconnecions inside the moule are listed here. The Timing signals from TFA+CFD block are routed through 100 ohm differential ECLlines for further processing. The detailed operartion priniples of various blocks briefed here can be obtained from individual technical reports prepared by the Electronics Laboratory.

The technical specifications, photographs, representative signals seen on CRO of Shaping Amplifier, TFA+CFD, ACOIN LOGIC UNIT are attached for references.

SPECIFICATIONS: CLOVER ELECTRONICS MODULE October 2003

ENERGY **4 SHAPERS with 3mS Shaping constant and fixed gain for 2* MeV/ 4 MeV/ 6 MeV.**
*** Default selection, Selected with 2 jumpers on PCB.**
Input and Outputs are accessed through LEMO connectors on Rear and Front panel respectively.

Controls for P/Z adjustment and BLR Threshold on Front panel.

Monitoring of BUSY and CLAMPED E_OUT (P/Z MON) possible through Front panel LEMO connectors.

TIMING **5 Timing Filter Amplifiers and Constant Fraction Discriminators for 4 clover detectors and ACS respectively.**

Timing Inputs are through Rear panel LEMO connectors.

WALK ADJUST, LLTH ADJUST, WALK MONITOR#, LLTH MONITOR on front panel.

TFA (attenuated) signal monitor for ACS is provided on front panel.

CFD outputs (F_NIM / 50nS & 500nS (ACS)) are available on rear panel.

PUR reject (TTL) available with 20uS moitoring period available on rear panel

ANTI-COINCIDENCE LOGIC UNIT

Accepts all required timing informations in ECL complementary logic levels from TFA+CFD units. The outputs and Monitors are provided on front panel through LEMO connectors.

The DELAY and WIDTH adjustments are possible on PCB.

MASTER GATE input (MGATE_IN) is TTL logic (positive) with "pull up" resistor.

POWER SUPPLY **The required power supply lines are filtered through ' pifilters. A -2Volts supply line for ECL termination is generated in a series pass zener regulator on board.**

CABINET **Double width NIM module**

SPECIFICATIONS SPECTROSCOPY AMPILIFIER*

Input Impedance	**~1000 ohm**
Pole/Zero adj.	**Input pulse having decay time about 50μSec ±5% can be corrected through potentiometer (FP) or remote controlled through DAC. Input impedance: 1K Control voltage not to exceed ± 1Volt.**
Shaping time & type	**~3 μSec. Fixed, Active integration (4th order) Quasi Gaussian having peaking time of 2.4τs.**
Input signal*	**-200mV/MeV is expected to generate +10 Volts at the output for 3 gain settings. Not to exceed ±10V.**
Gain	**2MeV, 4MeV and 6 MeV for +10V output. Jumper selection on board. Default is 2 MeV.**
BLR threshold	**Manual baseline restorer threshold is set through Potentiometer(FP) or remotely. Range is 0 to 600mV when provided. Impedance is 1k. Control voltage not to exceed ±10V**
Output	**Unipolar, Gated BLR DC restored. Width :~20μSec. Impedance 50 ohm**
BUSY	**A TTL negative logic pulse for the duration of presence of output pulse exceeds BLR threshold. Impedance: 10 ohm.**
PUR (optional)	**Pile up reject signal is a TTL positive logic signal, with pileup inspection interval of 20μSec. Impedance: 10 ohms.**
Power required*	**+/-6V, 40mA/20mA +/-12V 40mA/30mA +24V 5mA**
Size & Weight	**W x H x L : 1.75"x0.5"x 4", 30 grams.**
Technology	**Double sided PCB with PTH and SMD components are used.**

PERFORMANCES:

The module has been subjected to various tests at NSC with ^{60}Co and ^{152}Eu sources and in beam, in parallel with commercial modules. The typical results obtained are :

Resolution: 1.3KeV (122KeV), 2.0 KeV (1408 KeV) of ^{152}Eu @ 9 Kcps.

Integral non-linearity: ±80 eV for ^{60}Co spectrum .

Stability: With ^{60}Co, no significant shift observed at 6 kcps in 55 hours.

SPECIFICATIONS:	**TIMING FILTER AMPLIFIER***
INPUT IMPEDANCE	**50 ohms.**
GAIN(fixed)*	**~24(Ge)/15 (ACS)** **The input of -200mV/MeV is expected from Preamplifier.**
OUTPUT AMPLITUDE	**0 to ±2.5V into 50 ohm cable and load.**
OUTPUT IMPEDANCE	**~1 Ohm**
RISE TIME	**Better than 10nSec. With no additional integration across dynamic range.**
STABILITY (DC)	**Twin diode restorer used.**
POLE/ZERO ADJ.*	**P/Z internally corrected for 50μS (±5%) decay time internally.**
DIFFERENTIATION	**200nS (C1 X R12)**
INTEGRATION	**none. (R4 X Cx)**

*** For ACS, the P/Z network is wired for 400nS internally to match the decay time of BGO phosphor.**

SPECIFICATIONS: CONSTANT FRACTION DISCRIMINATOR*

INPUT SIGNAL	**Negative pulses accepted upto -5V**
THRESHOLD RANGE (LLTH)	**+60mV to -200mV Front panel adjustable.**
LLTH MONitor	**Measures x10 of actual LLTH set value.**
DELAY	**Internal, Zo: 100 0hm, 25nSec Fixed.**
FRACTION RATIO	**~ 0.3**
WALK ADJUST	**Front panel control for exact zero-cross voltage.**
WALK MONitor	**Front panel LEMO connector for monitoring CF signal.**
DEAD TIME	**~2 μS. (Fixed)**
WIDTH	**~50nS.(Fixed)**
OUTPUTS	**ECL DIFFERENTIAL 2 μS internal. ECL DIFFERENTIAL 50 nS internl. FAST NIM (2 nos.) 50 nS. Rear panel (optional)**
IMPEDANCE	**100 ohm DIFFERENTIAL ECL 50 ohm FAST NIM**
OTHERS	**SRT/CFD(Default) selection (Jumper on board)**
DIMENSION (WXHXL) & WEIGHT	**1.5" x 4" x 0.5", 50 grams**
TECHNOLOGY	**Both SMD and Through hole components used. Masked PCB 1.6mm/70μM Double sided with PTH.**

Note: For ACS, the same CFD daughter card is used without any dead time and output having width of 500 ηS.

SPECIFICATIONS: ANTI_COINCIDENCE LOGIC UNIT*

INPUTS (Internal) **ECL COMPLIMENTARY (Zo=100)**

CHANNEL A	**CFD 2 μS DEAD TIME**
	CFD 50 nS. width
CHANNEL B	**CFD 2 μS DEAD TIME**
	CFD 50 nS. width
CHANNEL C	**CFD 2 μS DEAD TIME**
	CFD 50 nS. width
CHANNEL D	**CFD 2 μS DEAD TIME**
	CFD 50 nS width
AC SHIELD	**CFD 500 nS width**

MASTER GATE (MGATE_IN)

TTL (positive) internally pulled up input.
Must arrive within 1μS/2μS of individual CFD outputs.

OUTPUTS

ANTI-COINCIDENCE (A_COIN) **FAST NIM (Front panel LEMO)**
WIDTH 500 nS. (adjust on BOARD)
After "OR"ing of CFD (50 ns) outputs from channels A to D "DELAY"ed by ~100 nS. GATED with ACS (500 nS) for Coincidence and output is generated.

START/STOP(TDC) **FAST NIM (Front panel LEMO)**
WIDTH 50 nS
After Coincidence, the signal is DELAYED (200 nS-800 nS Adjusted on BOARD) and output is generated.

MONITOR(OR_P) **F_NIM (Front panel LEMO)**
The CFD (50 nS) outputs are logic ORed and Level converted and shaped(100nS).

ADC GATEs(GATE A-D) **Positive TTL (Front panel LEMO)**
Zo: 10 ohms. WIDTH 10 μS.
Refer to Block diagram. Generated only when Master_Gate is present within 1μS of the input signal.

PUR SUM(PUR A-D) **POSITIVE TTL (Rear panel LEMO)**
PUR inspection WIDTH 20 μS
Zo: 10 ohms. It is "OR" of four piled up channels.

DIMENSION **4 " x 0.5" x 3.75" 80 grams. W x H x L**

NOTE: * Refer individual technical report for details.

Gain Selection Procedure:

The Shaper is designed to work with one of the three different GAIN settings 2MeV*/4MeV/6MeV as per user requirement. The GAIN can be selected on the SHAPER daughter card by the procedure given here.

Open the side panel of Clover Electronics Module

1. Locate the SHAPERS in TOP of Mother Board.
2. Identify JUMPER SOCKETS in extreme right corner facing top. (Ref. Photograph)
3. By plugging 'i'nany on the jumper will select 4MeV.
4. By plugging 'i'nboth jumpers will select 6MeV.

   * Default GAIN selection when jumpers are not used.

We suggest the user not to plug out the daughter card for GAIN change. Instead use fingers/sharp nose pliers to plug in/out jumper headers for gain change.

Pole_Zero Adjustment:

The Shaper is designed to work with Eurisys Measures Clover detectors with preamplifiers having 50µS (±5%) decay time constant. The Pole_Zero adjustment can be done with front panel PZ_Adj. Potentiometer while monitoring corresponding front panel PZ_ Mon. on a CRO. Any major deviation (above ±5%) in decay time can be corrected in Preamplifier card as suggested by the manufacturer.

BLR Adjustment:

The Shaper is designed to have stable zero reference at all specified working conditions. This is achieved by Gated BLR operation. The required threshold level above system noise is fed through front panel BLR adj. potentiometer. This is set while monitoring front panel BUSY (TTL) signal on a CRO for a minimum count rate when no radiation sources are used. It is essential to set proper Pole Zero adjustment for proper functioning of BLR. During above procedures, it is recommanded to use corresponding BUSY signal to trigger CRO.

Schematic Diagram

For easy references, a set of circuit diagrams are attached. The circuit diagram of individual blocks can be obtained from Electronics laboratory, NSC. The entire mother board is mounted on side rails of a double width NIM module. The individual blocks are assembled in daughter card form and plugged into low profile machine trimmed sockets. The front panel trimmer potentiometers (3006P) are hood mounted. The series pass regulator transistor is electrically isolated and mounted on rear panel for heatsinking.

Assembly Procedure

The currently (MOTHERBRD_PT2, OCT_2002) available PCB is of glass epoxy, double sided with 0.6mm drill PTH having dimension of 7.25" x 8.5". It is recommended to have solder mask and silk screen printed on both sides for easy assembly as well to protect it from solder bridges etc.,. Use of 0.2mm sharp solder tip, IC solder tips are recommended in order to solder narrowly spaced SMT devices. SMT devices shall be picked only by fine quality tweezers. While soldering a magnifier x5 (large) and x12 (eye piece) is used to assure the soldering. It is essential to use solder cleaning liquid with cotton swab to remove dust attracting solder paste.

The PCB shall be checked with magnifiers and multimeter for any unwanted connections and PTHs. Then components shall be soldered in a orderly manner, to start with all low profile chip resistors and capacitors. It is essential to check the impedance between various nodes after soldering resistors, capacitors and inductors. Active components like diodes, transistors and ICS are soldered thereafter. At last tantalum capacitors, connectors, jumpers and any non-SMT devices. All PCBs shall be marked distinctly with unique number for any future references. The Series pass transistor is mounted in conventional way with heatsink kit.

Reference:

1. Electronics for INGA at NSC by Dr.R.K.Bhowmik

Assembly Procedure:

Check for any solder bridge with Magnifier lamp + magnifier eyepiece (x10/x12) as well as with multimeter. Known solder bridges in this PCB are listed in this maual. Apply thin flux for good solder connection (No clean solder flux recommanded). Assemble the pins first carefully flush mounted, with great care to avoid any solder bridges and excess solder. Assemble the resistors and capacitors 0805 footfrint and SOT123 active parts like diodes. Capacitors (polarised) and Fuses would be followed with RFCoils wound as per instructions given in schematic. Remaining errors related to Diodes and capacitors in Shaping Amplifiers and additional DC blocking capacitor for ACS TFA shall be corrected.

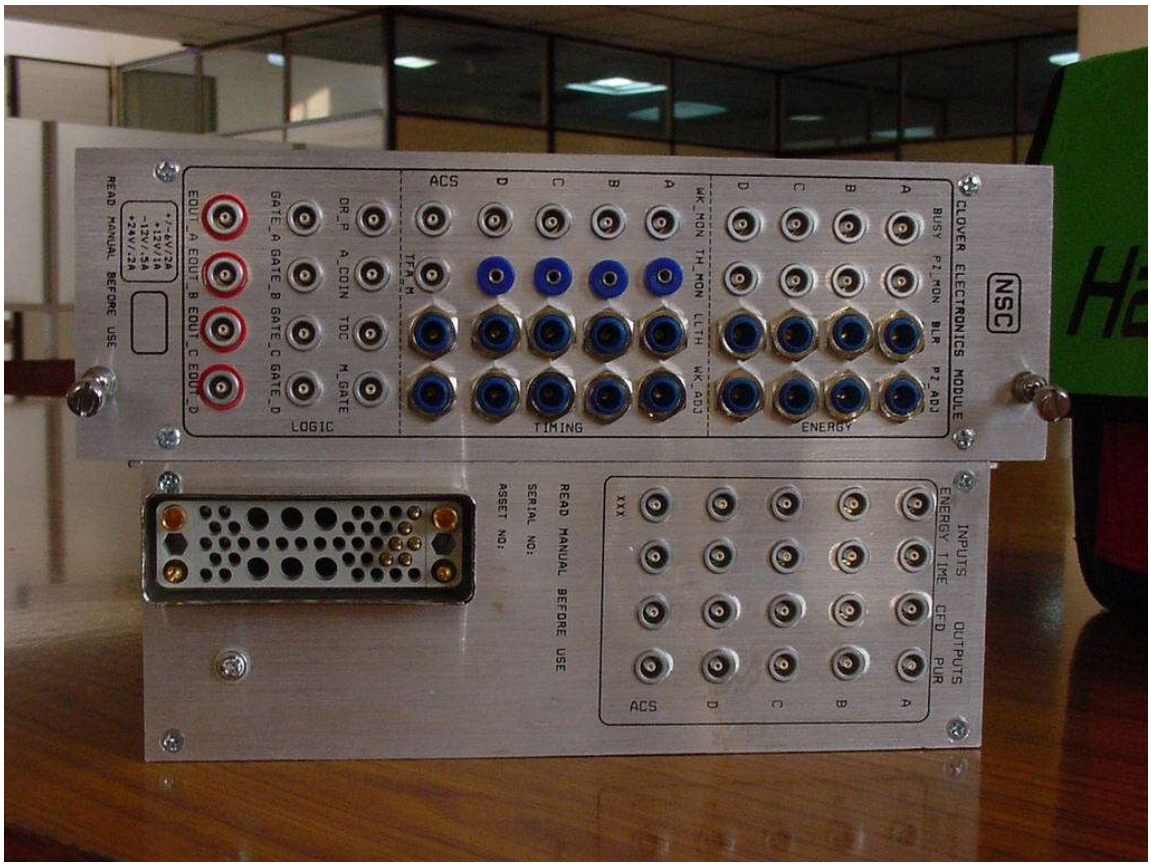
Check again with magnifier for any solder bridges and shorts with multimeter. Clean the PCB with good Pcb cleaner and cotton for any excess Flux which attracts dust during long operation. Check the mother board with DC power supply and multimeter for working of M2V supply line and power supply distribution to all daughter cards.

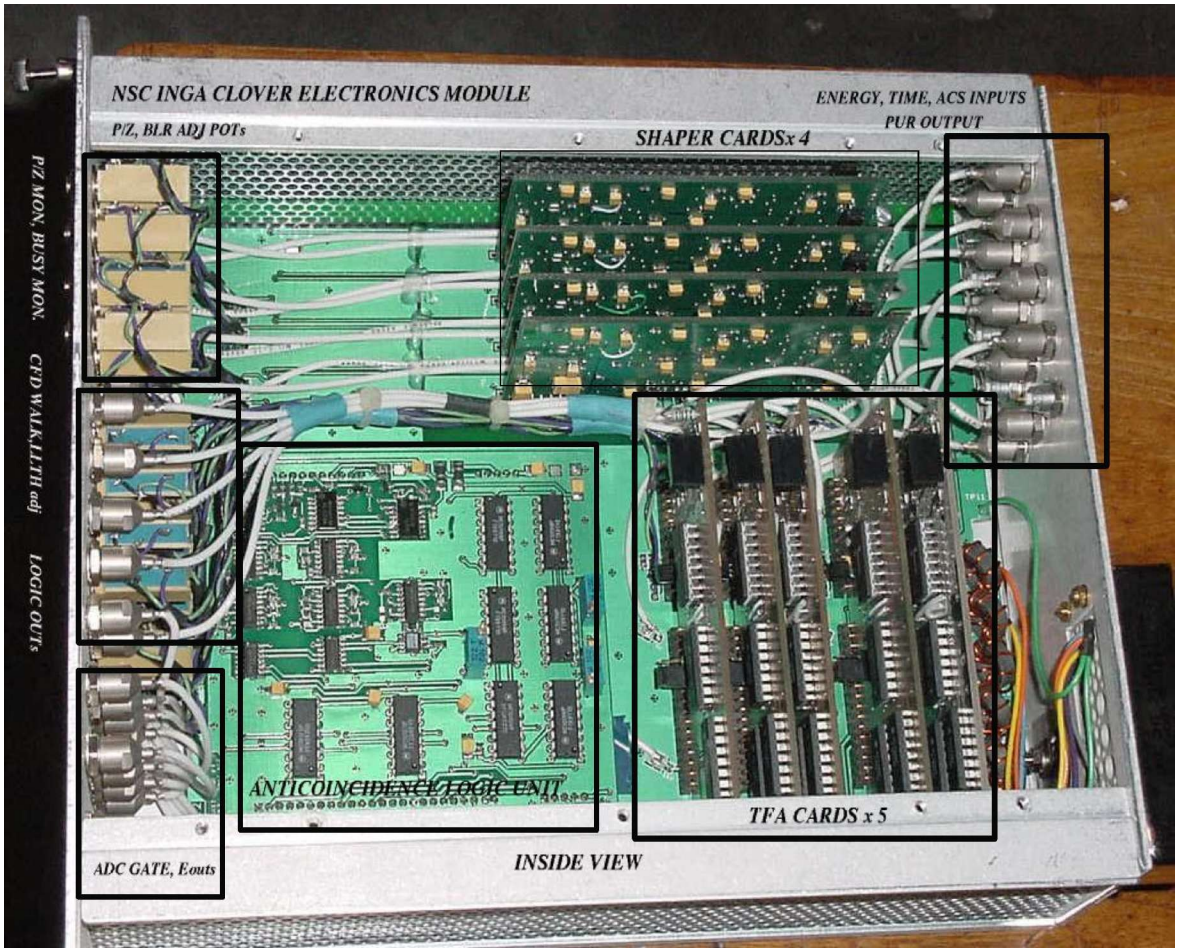
Preparation of Cabinet:

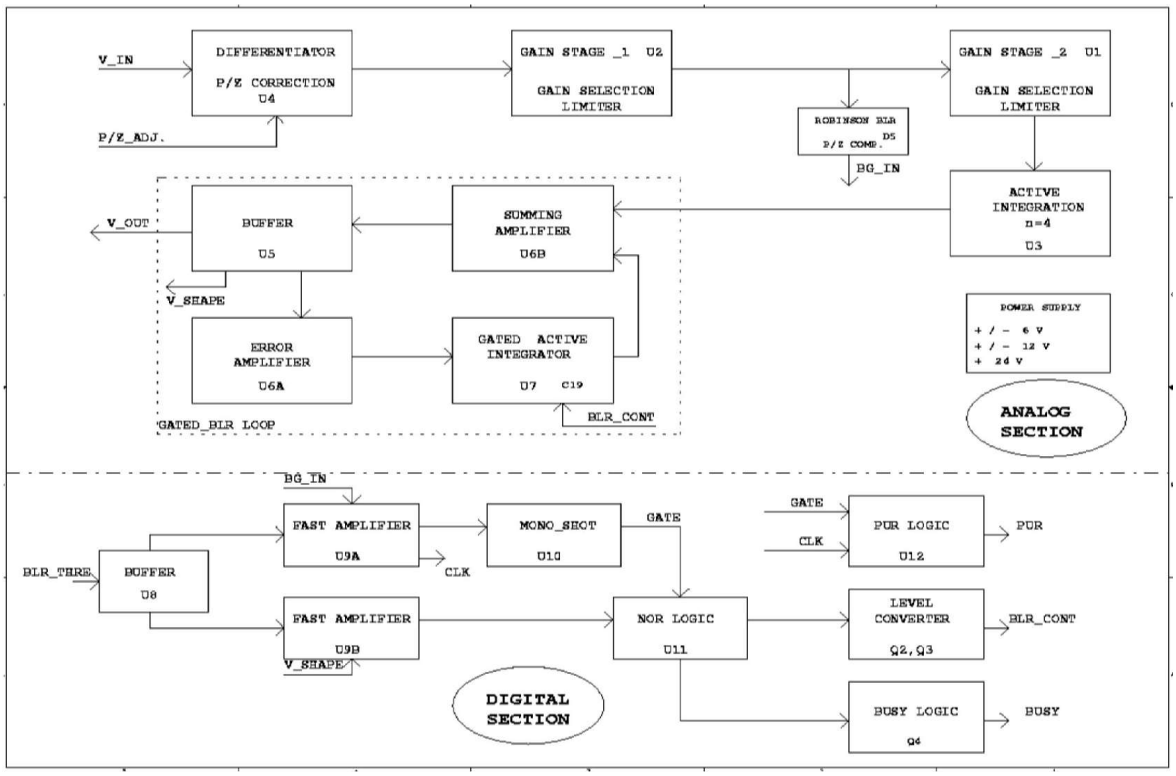
The double width cabinet of NIM standard is used as housing for this module. The mother board Pcb shall be placed on the rails inside the cabinet for proper sizing before fixing it. Excess projection of PCB shall be removed with "Rough File" before component assembly. The front panel and back panel punch details are given in this manual and punching shall be done with great to avoid wastage of cabinet assembly. The screen printing can be done after punching of the panels. The sample screen print schematic is also attached here. The PCB is secured on the side rails with four numbers of 4-40 size 1/4inch pan head screws on tapped holes.

Wiring:

The standard lengh of 3 core flat wire and RG178C/U used for interconnections inside the module are listed for easy assembly. Good hand tools and neat assembly procedure shall be followed for any maintenance free operations. The connections invloving coaxial cables shall be done first and followed by potentiometer connections. Confirm the wiring also with good quality continuty checker (multimeter). While mounting the LEMO connectors and potentiometers, avoid any scratch to front and rear panels, and use standard tools for quality finishing. The wiring orientations shall be checked while powering the unit with daughter cards and necessary wiring correction shall be done incase of any reversal.


CLOVER ELECTRONICS MODULE
NSC
ACS
LOGIC
TIMING
ENERGY
READ MANUAL BEFORE USE
INPUTS
OUTPUTS


NSC INGA CLOVER ELECTRONICS MODULE
P/Z, BLR ADJ POTs
SHAPER CARDSx 4
ENERGY, TIME, ACS INPUTS
PUR OUTPUT
P/Z MON, BUSY MON
CFD WALK,LLTH adj
LOGIC OUTs
ANTICOINCIDENCE LOGIC UNIT
TFA CARDS x 5
ADC GATE, Eouts
INSIDE VIEW


V_IN
DIFFERENTIATOR
P/Z CORRECTION
U4
P/Z_ADJ.
GAIN STAGE _1 U2
GAIN SELECTION
LIMITER
ROBINSON BLR
P/Z COMP. DS
BG_IN
GAIN STAGE _2 U1
GAIN SELECTION
LIMITER
ACTIVE
INTEGRATION
n=4
U3
V_OUT
BUFFER
U5
SUMMING
AMPLIFIER
U6B
V_SHAPE
ERROR
AMPLIFIER
U6A
GATED ACTIVE
INTEGRATOR
U7 C19
BLR_CONT
GATED_BLR LOOP
POWER SUPPLY
+ / - 6 V
+ / - 12 V
+ 24 V
ANALOG
SECTION
BG_IN
FAST AMPLIFIER
U9A
MONO_SHOT
U10
GATE
CLK
BLR_THRE
BUFFER
U8
FAST AMPLIFIER
U9B
V_SHAPE
NOR LOGIC
U11
GATE
CLK
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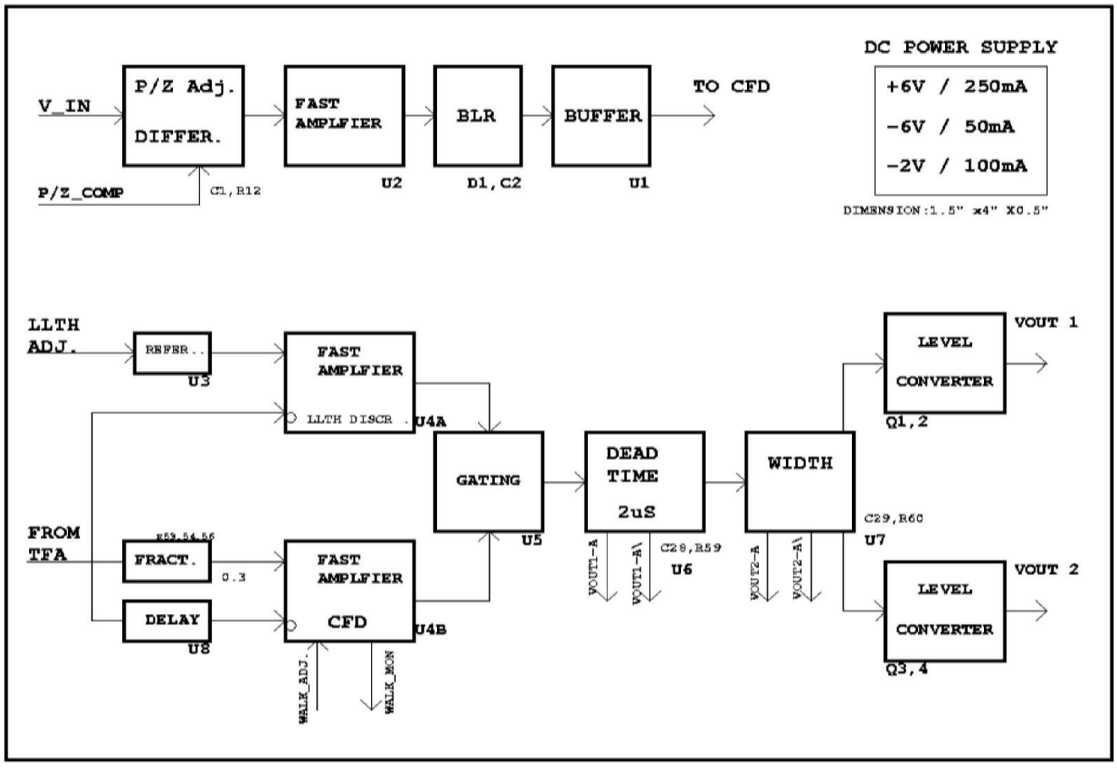
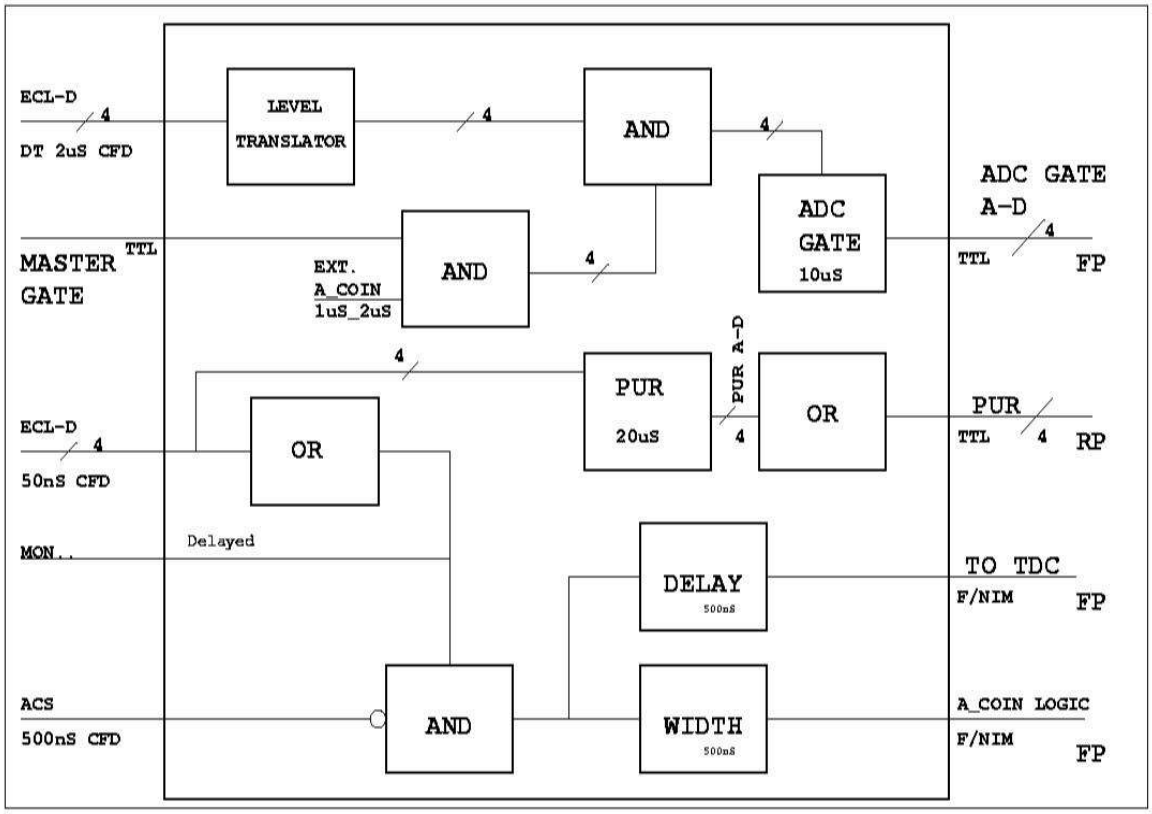
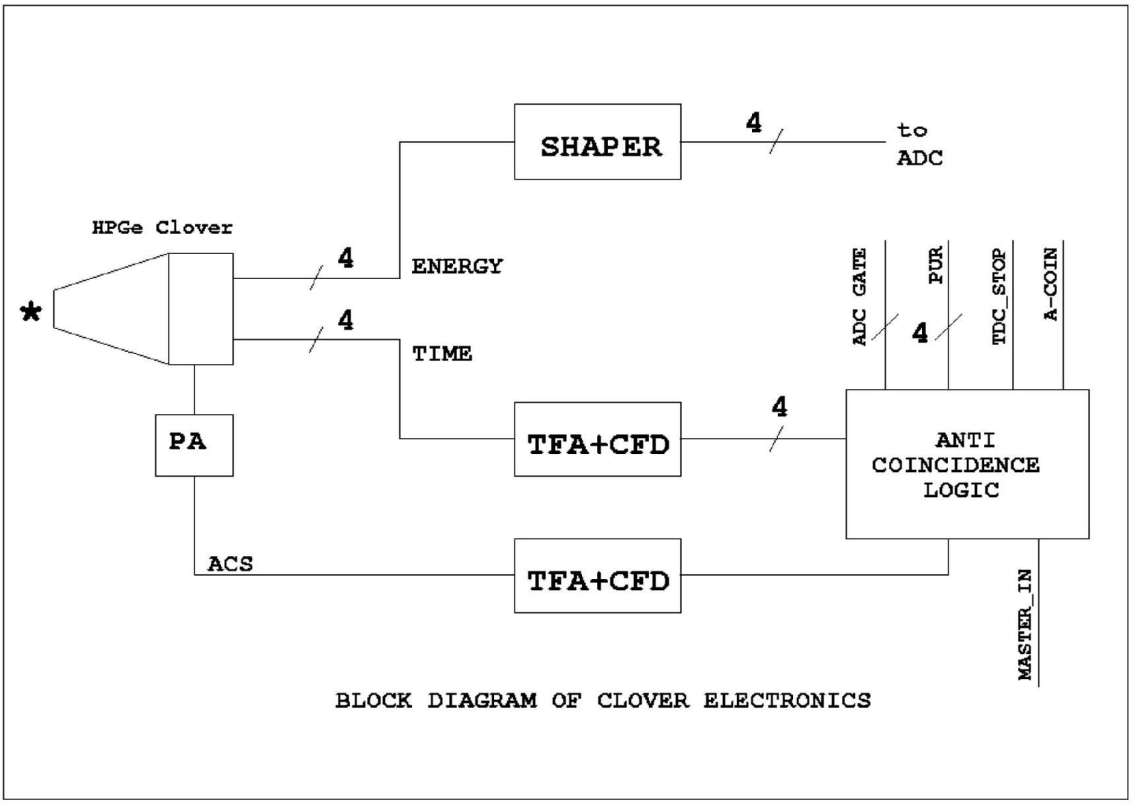
BUSY LOGIC
Q4
BUSY
DIGITAL
SECTION


DC POWER SUPPLY
+6V / 250mA
-6V / 50mA
-2V / 100mA
DIMENSION:1.5" x4" X0.5"
V_IN
P/Z Adj.
DIFFER.
P/Z_COMP
C1,R12
FAST
AMPLFIER
U2
BLR
D1,C2
BUFFER
U1
TO CFD
LLTH
ADJ.
REFER..
U3
FAST
AMPLFIER
LLTH DISCR.
U4A
GATING
U5
DEAD
TIME
2uS
U6
WIDTH
C29,R60
U7
LEVEL
CONVERTER
Q1,2
VOUT 1
FROM
TFA
R53,54,56
FRACT.
0.3
DELAY
U8
FAST
AMPLFIER
CFD
U4B
C28,R59
LEVEL
CONVERTER
Q3,4
VOUT 2
WALK_ADJ.
WALK_MON





BLOCK DIAGRAM OF CLOVER ELECTRONICS