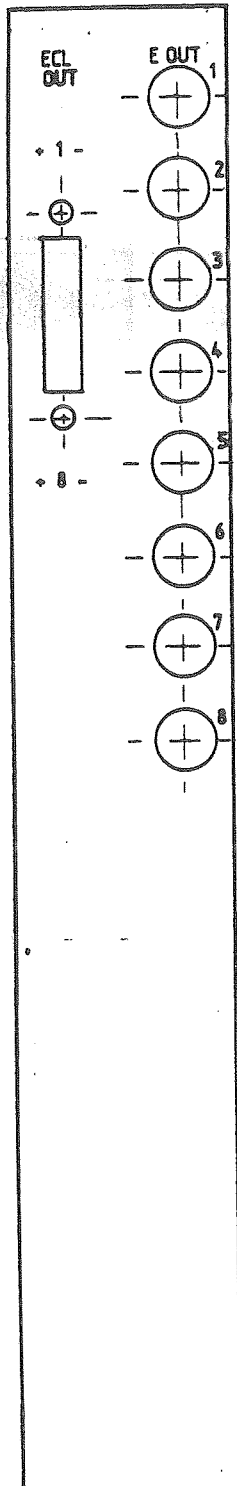


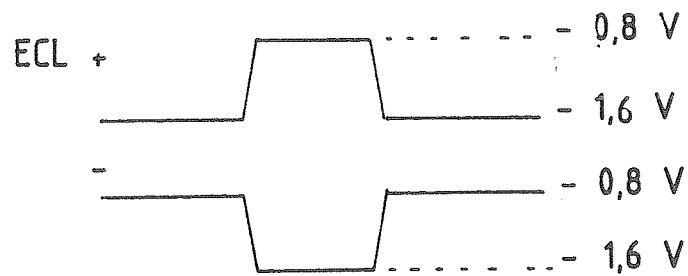
CF 8000

(REAR PANEL)



ANALOG OUT (AC COUPLED)

OUT B; WIDTH= TB



DIFFERENTIAL LINE
LINE IMPEDANCE : $112. \Omega$

DELAY TIME : 2,4, 10 ns
USING 10 ns HYBRID DELAY PLUG IN

AVAILABLE ALSO :
6,12, 30ns (30 ns PLUG IN)
10,20,..... 50ns (50 ns PLUG IN)

CF 8000

OCTAL CONSTANT FRACTION DISCRIMINATOR

Specifications:

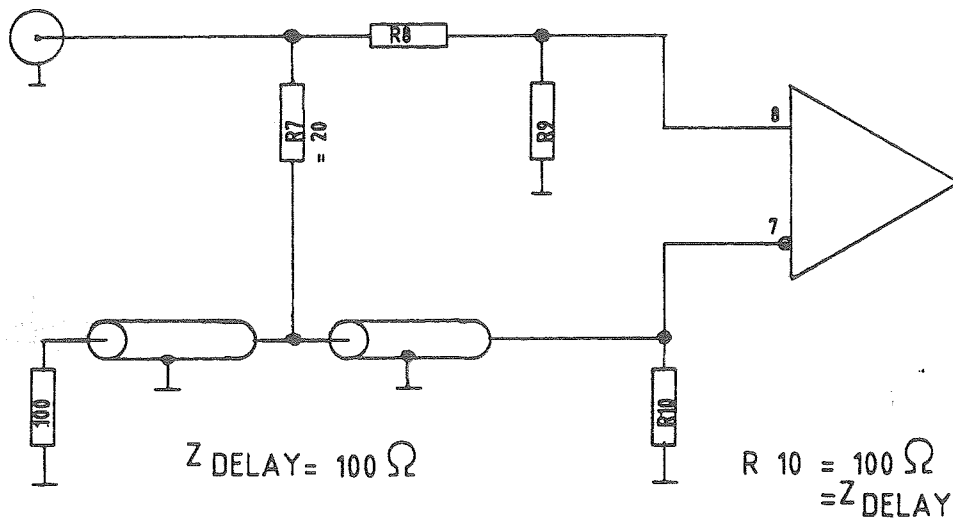
- 8 channels in a single width module
- fraction 0.2 on a resistor-network plug in;
other fractions possible
- DC-coupling throughout for high countrate capability
- wide dynamic range of input signals
(- 0mV to - 3V)
- threshold (of leading edge discriminator)
adjustable from 0 to 1 Volt independently for
every channel (caution: if threshold is between
0 and 30mV, coupling from one channel to the
neighbouring channels may occur)
- testpoint on the frontpanel to monitor the
threshold voltage for every channel
- internal hybrid-delay plug in; no external cabling
necessary

hybrid circuits for a delay of 2 to 10 ns, 5 steps,
6 to 30 ns, 5 steps and 10 to 50 ns, 5 steps are
available
- automatic walk adjust using a gated baseline restorer
(operational amplifier). No manual adjust necessary
- Dynamic range > 500 : 1
- walk less than \pm 500 psec
- dead time = T_A adjustable on the frontpanel
once per module (20ns200ns)
- second time constant T_B adjustable on the front panel
once per module (20ns200ns)

- four outputs per channel
 - one FAST NIM OUT (- 20mA in 50 Ω)
 - width = T_A = deadtime (updating)
 - two FAST NIM OUT (2*(-20mA) in 50 Ω)
 - width = T_B
 - one ECL differential-line OUT on the rear panel
 - 2 x 8 pin connector, width = T_B
- one AC-coupled ANALOG OUT per channel on the rear panel (Attenuation = 1:2)
- Common INHIBIT input: disables outputs B
 - FAST NIM, 50 Ω terminated, threshold = -0.4V
- Multiplicity output, analog signal width = T_B
 - amplitude = number of triggered channels times 50mV
- common OR output (FAST NIM, - 20mA in 50 Ω)
 - output signal, when one channel triggers
 - width = T_B
- analog sum of input signals
 - (attenuation 1:20...)

CF 8000

SELECTING FRACTION



$$1.) 70 \Omega \parallel (R_8 + R_9) = 50 \Omega$$

$$R_8 + R_9 = 175 \Omega$$

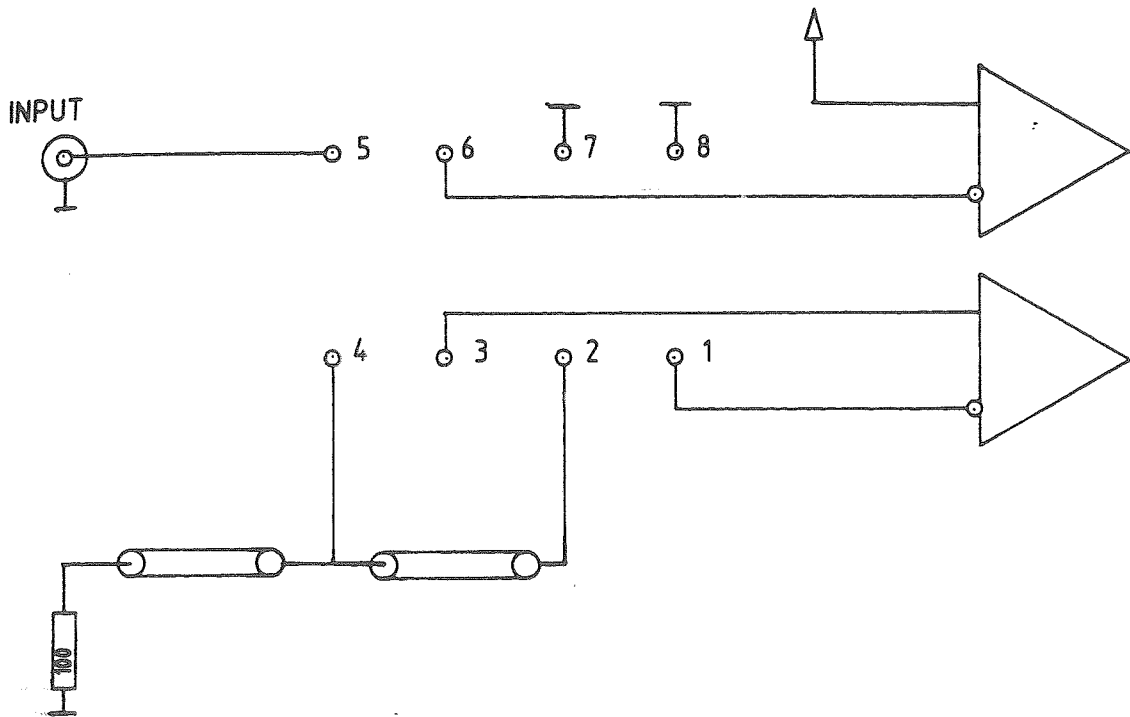
$$2.) R_9 = 175 \Omega \cdot \frac{50 \Omega}{70 \Omega} \cdot f = 125 \times f$$

$$R_8 = 175 - R_9$$

$f = 0,2$

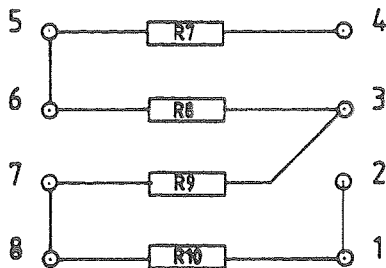
$f = 0,4$

		$f = 0,2$	$f = 0,4$
R7 =	20 Ω	20 Ω	20 Ω
R8 =	175 Ω - R9	150 Ω	125 Ω
R9 =	125 Ω x f	25 Ω	50 Ω
R10 =	100 Ω	100 Ω	100 Ω



A. TO CHANGE THE FRACTION

RESISTORS R3 AND R4 HAVE TO BE CHANGED USING THE FOLLOWING RELATION



CF

FRACTION = f

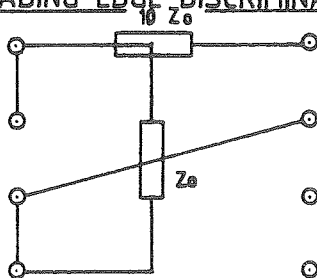
$R7 = 20 \Omega$

$R10 = 100 \Omega$

$R8 = 175 \Omega - R9$

$R9 = 125 \Omega \cdot f$

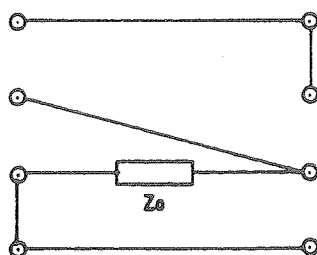
B. USING CF 8000 AS A LEADING EDGE DISCRIMINATOR



LE

$Z_0 = 50 \Omega$

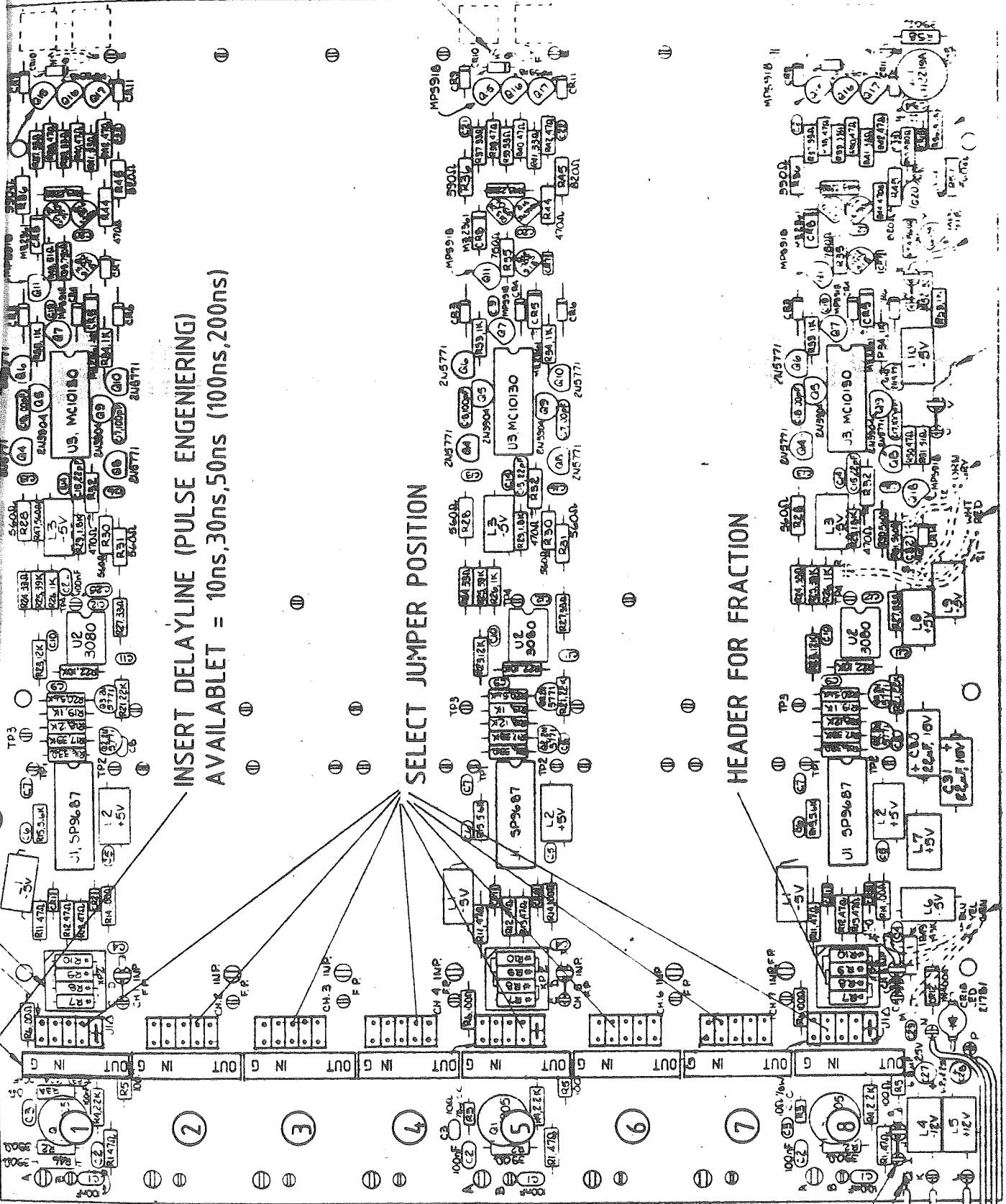
C. USING CF 8000 AS A ZERO CROSSING DISCRIMINATOR



Z/C

$Z_0 = 50 \Omega$

FRONT PANEL



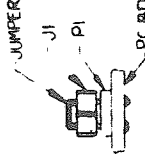
INSERT DELAYLINE (PULSE ENGINEERING)
 AVAILABLET = 10ns,30ns,50ns (100ns,200ns)

SELECT JUMPER POSITION

HEADER FOR FRACTION

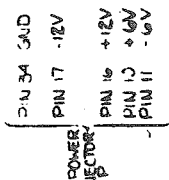
REAR PANEL

5/5 T	1
4/5 T	1
3/5 T	1
2/5 T	1
1/5 T	1



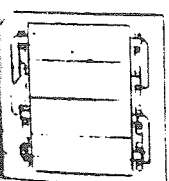
PC BD.

AX TO 2
 MANECTOR (FP)
 DDER TO GROUND
 PLANE



SOLDER RESISTORS
 AS SHOWN

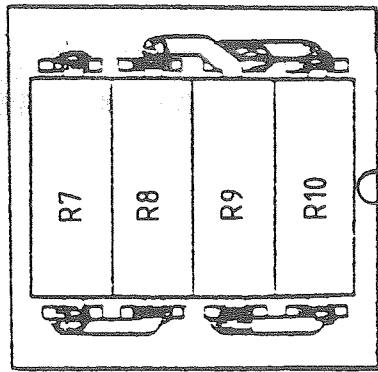
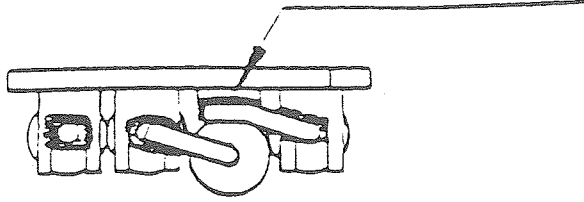
DETAIL A
 SCALE 4:1
 TYP. 8 PLCS



CF 8000

FRACTION PLUG IN

SOLDER RESISTORS
AS SHOWN



SOLDER RESISTORS
AS SHOWN.

DETAIL A

SCALE: 4:1
TYP. 8 PLCS

Testprozedur CF 8000

Gerät: NIM-Crate mit ± 6 V,

Pulsgenerator: 2ns Anstieg -2 V

30 ns breit

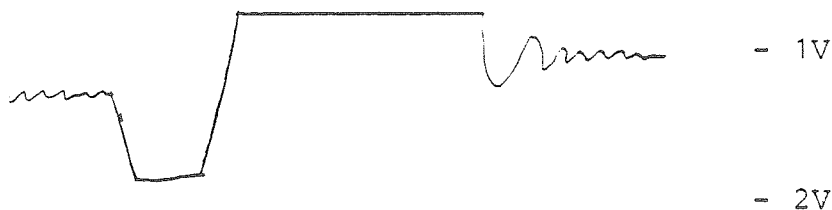
entspr. Oszillograph (kann von GSI bereitgestellt werden)

1. Gerät einstecken, Ströme messen:

-6 V : 1,15 A, + 6V : 250mA, - 12V : 40mA, + 12V : 40mA

2. TH Trimmer durchdrehen und dabei an Testpunkt Spannung messen. Spannung muß sich zwischen 0 V und ca. -0.9 bis -1 V variieren lassen. Spannung dann überall auf 100 mV einstellen.

3. Puls mit 2 nsec Anstiegszeit, 2 V Amplitude und 10 ns Breite an LN Buchse (rate ~ 1 MHz). Puls an TP 2 muss "symmetrisch" aussehen. (8x)



4a. Width-Trimмер TA durchdrehen und dabei 1 Ausgang (A) ansehen; Breite soll von 15 ns bis 250 ns variieren, dann Breite auf 100 ns einstellen.

4b. Width-Trimмер TB durchdrehen, 1 Ausgang (B) ansehen; Breite soll von 15 ns bis 250 ns variieren, dann Breite auf 50 ns einstellen.

5. Alle OUT Buchsen ansehen: 8x A, 16x B.

$t_A \approx 100$ ns $t_B \approx 50$ ns



6. Test Σ out: Signal auf Eingang 1 geben, an Σ out muß Eingangssignal abgeschwächt sichtbar sein (Kabel mit 50 Ω abschließen) dgl. Eingang 2 bis 8

7. Test OR out: Signal auf Eingang 1 geben; an OR out muß Signal der Länge TB sichtbar sein



(Neg. NIM)

(Kabel mit 50 Ω abschl.)

dgl. Eingang 2 bis 8

8. Test M out: Signal auf Eingang 1 geben; an M out muß abgeschwächtes neg. Signal (... mV) sichtbar sein (Länge TB) (Kabel mit 50 Ω abschließen)

dgl. Eingang 2 bis 8

9. Test INH IN: Signal auf Eingang 1 geben, an Ausgang 1B erscheint Signal

Auf INH IN -0.8 geben (Modul wird bereitgestellt)

Signal verschwindet

dgl. Eingang 2 bis 8

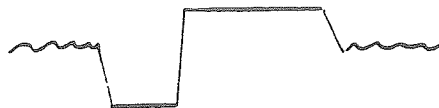
10. Test ANALOG out: Signal auf Eingang 1 geben; an Analog out 1 erscheint Eingangssignal

dgl. Eingang 2 bis 8

11. Test der Delays:

Signal auf Eingang 1 geben TP2 (Kanal 1 ansehen)

Signalform



Steckbrücke auf Position 1 (unten) $t = 2\text{ns}$

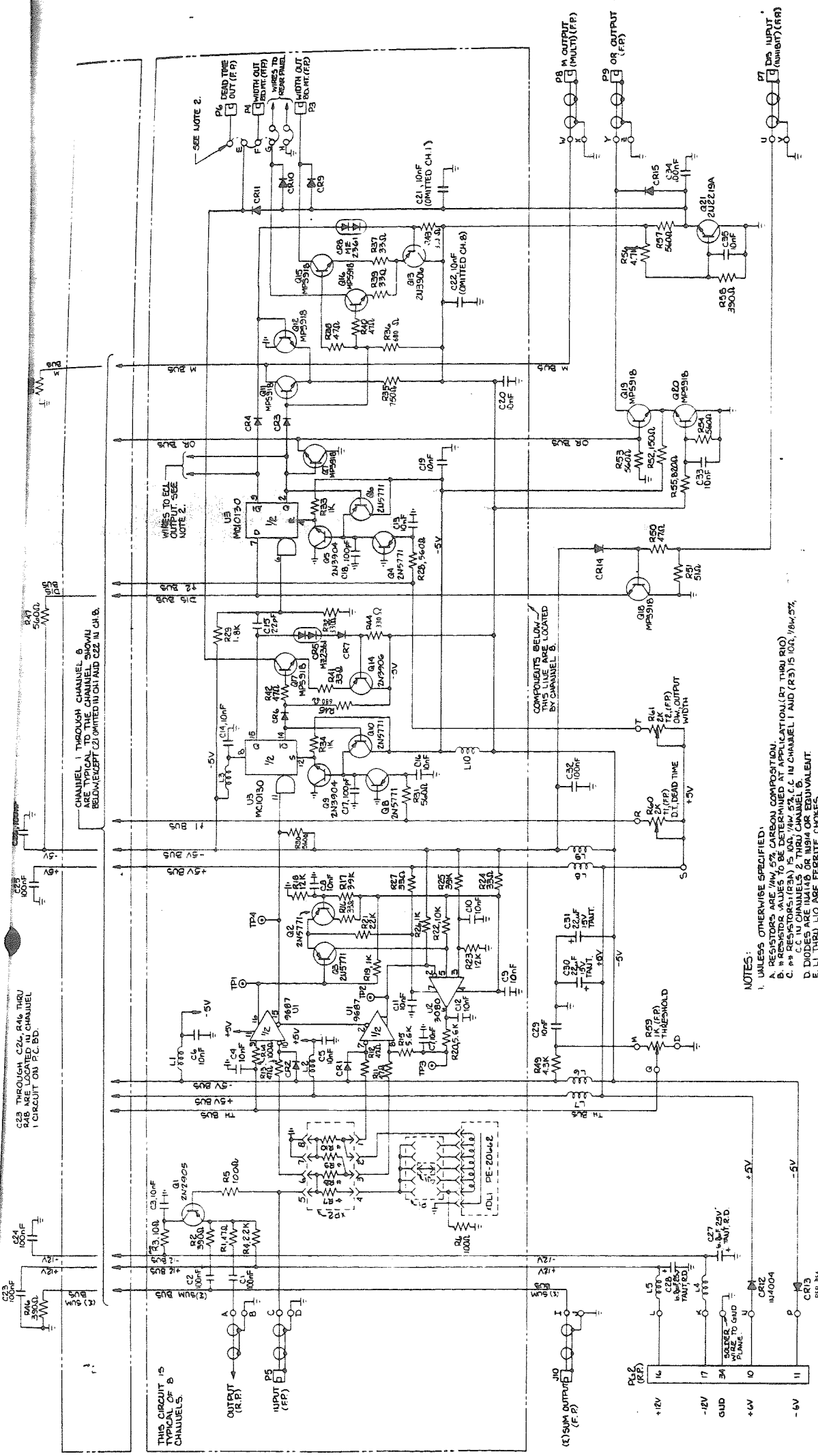
" 2 $t = 4\text{ns}$

usw. ...

5 $t = 10\text{ns}$

dgl..Kanal 2 bis 8

12. TEST ECL Ausgänge: ECL Ausgang verbinden mit ECL-NIM-Converter(z.B. ECL 1601) Signal auf Eingang 1 geben.An NIM -Ausgang des Converters muß Signal der Länge T_B sichtbar sein.



CF 8000

OCTAL CONSTANT FRACTION TRACKER BOARD	
REV.	DATE
1	10/17/67
2	11/1/67
3	11/1/67
4	11/1/67
5	11/1/67
6	11/1/67
7	11/1/67
8	11/1/67
9	11/1/67
10	11/1/67

REV.	DATE	BY	CHKD.
1	10/17/67	J. L. MAIER	
2	11/1/67	J. L. MAIER	
3	11/1/67	J. L. MAIER	
4	11/1/67	J. L. MAIER	
5	11/1/67	J. L. MAIER	
6	11/1/67	J. L. MAIER	
7	11/1/67	J. L. MAIER	
8	11/1/67	J. L. MAIER	
9	11/1/67	J. L. MAIER	
10	11/1/67	J. L. MAIER	

SCHEMATIC
 DRAWN BY: J. L. MAIER
 CHECKED BY: J. L. MAIER
 DATE: 11/1/67
 BOARD NO: 21X612A 5-A

- NOTES:
- UNLESS OTHERWISE SPECIFIED:
 - RESISTORS ARE 1/4W, 5% CARBON COMPOSITION
 - RESISTOR VALUES TO BE DETERMINED AT APPLICATION (RT THRU RIO)
 - ** RESISTORS (R2A) IS 100, 1/4W, 5% C.C. IN CHANNEL 1 AND (R3) IS 100, 1/4W, 5% C.C. IN CHANNEL 2, THRU CHANNEL 3.
 - DIODES IN CHANNELS 2, THRU CHANNEL 3.
 - L1 THRU L10 ARE FERRITE CORES EQUIVALENT.
 - Δ J1 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J2 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J3 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J4 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J5 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J6 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J7 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J8 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J9 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - Δ J10 PLACEMENT IN P1 TO BE DETERMINED AT TIME OF APPLICATION.
 - JUMPERS SHOWN IN A DASHED LINE ARE FOR VERSION A; JUMPERS SHOWN IN A SOLID LINE ARE FOR VERSION B; NO JUMPERS WITH WIRES FROM U3 PINS 2 AND 5 GOING TO ECL OUTPUT (R,P) ARE FOR VERSION C.
 - DESIGNATORS COMMON TO ALL 3 CHANNELS ARE: R1 THRU R45, C1 THRU C22, U1 THRU U5, TP1 THRU TP4, AND A THRU H.
 - REFERENCE DRAWINGS: 21X612A C-1 PARTS LIST
 21X612A C-1 P.C.B.D. ASSEMBLY

REF.	DESCRIPTION	UNIT USED	NOT USED
U1	TP4		
L10	L10		
U3	U3		
DL1	DL1		
CR15	CR15		
G21	G21		
C35	C35		
R61	R61		
U5	U5		
U4	U4		
U3	U3		
U2	U2		
U1	U1		

REF.	DESCRIPTION	UNIT USED	NOT USED
P10	P10		
P9	P9		
P8	P8		
P7	P7		
P6	P6		
P5	P5		
P4	P4		
P3	P3		
P2	P2		
P1	P1		